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TELECOMMUNICATIONS

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BULK ACOUSTIC WAVE FILTERS FOR IF PROCESSING IN RADIOCOMMUNICATION SYSTEMS

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The civil radiocommunication market has been caracterized by two main changes in the recent years :

- the expansion of digital communication

- the increase of the market with the emergence of new high volume applications such as GSM, DCS, POINTEL in Europe and comparable services in USA and Japan.

This leads to significant changes in the piezoelectric filter market.

Previous analog systems required a narrow band IF filtering (typical channel width : 15 kHz). The conveniant filter is normally realized with quartz resonators and capacitive coupling. It is quite tolerant to manufacturing conditions.

Digital systems need a larger bandpass (in a range 50 to 300 kHz). So the filter is at the boundary of the quartz range of use ; it becomes a high performance filter both on theoretical and technological point of view.

It is a major change because it has numerous consequences on the design of the filter and on the process of manufacturing. It even affects the choice of piezoelectric material.

IF filtering in systems :

The question of IF filtering is shared by both the mobile and the base station. The electrical requirements are quite the same. However there are significant differences regarding non electrical characteristics and, of course, price and volume target.

The manufacturer of system generally may choose whether one or two IF stage is needed for radioprocessing. The requirements for the shape of each filter is the result of the splitting of a global need over the two IF filters.

IF frequencies may usually be selected in the following ranges :

- 20 to 200 MHz for the first IF with focus on 45, 70, 85 MHz
- 10.7 to 45 MHz for the second IF.

Whatever may be the centre frequency and the channel width, there is a common need for the global filtering shape over the following characteristics :

- shape factor must be approximately 3 : 1 between attenuation level -3 dB and -60 dB. It is an equivalent 6 pole filter which may be split between a two pole and a four pole at each IF frequency

- group delay must be flat in the limit of 15 % of its absolute value over 60 % of the 3 dB bandwidth

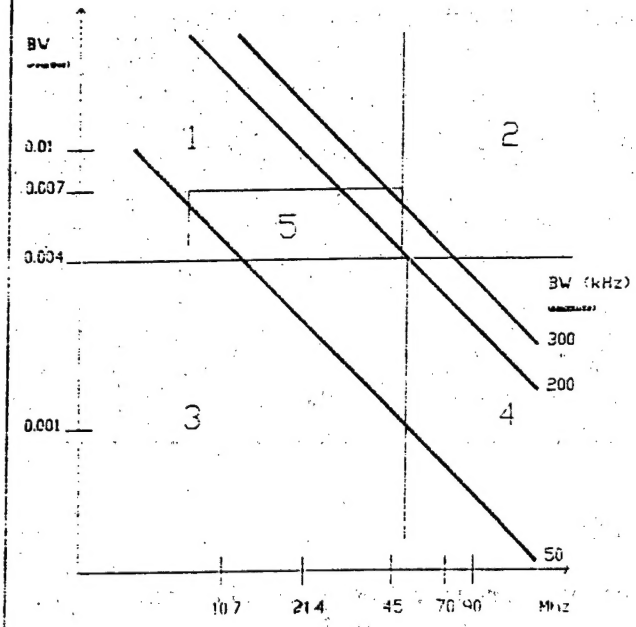
- insertion loss must be as low as possible, especially for mobile stations where low consumption is a main deal. 8 dB split over two filters seems to be a maximum

- an out of band rejection of 80 dB is needed to avoid effects of near jammers

- size must be as small as possible for mobile stations

- cost is obviously a main parameter

Even so, the various combinations of centre frequencies and bandwith lead to very different filter designs because the need is at the boundary of different technological domains. (fig.1)



Legend for the domains

1. Lapped lithium tantalate
2. Ion etched lithium tantalate
3. Lapped quartz
4. Ion etched quartz
5. Special mobile technology (low size - low cost)

Fig. 1
Technological domains of crystal filters and locus of radiocommunication bandwidths

We will focus on the products developped for GSM system, because this system has been the earliest one.

I/ FILTERS FOR GSM

A/ BASE STATION

CEPE has developped a range of filters for the GSM base stations with the following characteristics :

centre frequency Fc :	60 to 90 Mhz
Shape factor :	4 poles
3 dB bandwidth :	from 130 kHz to 200 kHz
Stopband attenuation :	20 dB min out of Fc ± 200 kHz
	60 dB min out of Fc ± 600 kHz
Out of band rejection :	70 dB min
Insertion loss :	5 dB max
Group delay ripple :	1 μs max over 60 % of the 3 dB bandwidth
Spurious rejection :	40 to 65 dB min (depending on bandwidth)
Continous input level :	-2 dBm
Temperature range :	-20 to +70°C
Package size :	38 x 18 x 15 mm (fig. 2 - right)

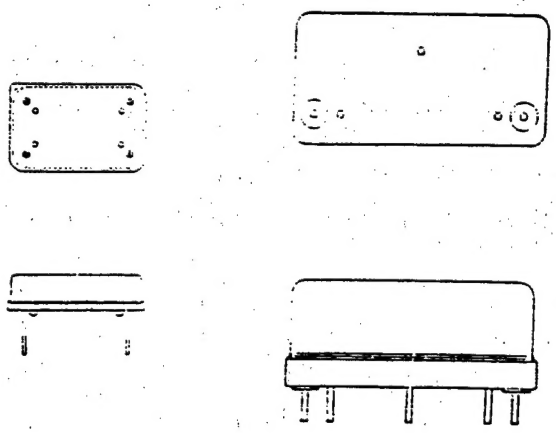


Fig. 2
Package for mobile (left) and base (right) filters

The main technical choices have been :

- resonators are working at fondamental frequency. It is impossible to use harmonics due to the large relative bandwidth ($> 4.10^{-3}$).
  As the centre frequency exceeds the limits of mechanical lapping (which is approximately 50 MHz) the resonators need to be ion etched (resonator thickness : 18 μm). This technology has been mastered by CEPE for 15 years and is well suited for reproducible medium volume manufacturing of resonators.

- quartz has been chosen as piezoelectric material, even if the relative bandwidth is quite large compared to the small piezoelectric coupling factor. But, lithium tantalate which has a stronger coupling factor would not have been satisfactory regarding insertion loss and stiffness, due to its poor quality factor.

The consequence is a high level of iterative impedance and the need for coils with high quality factors.

- other aspects of the filters are the common state of the art at CEPE which have been performed on manufacturing of comparable volume in the recent years (ex : MSE RITA > 15 000 filters).

In order to face this new production and to continue facing it in the following years, very significant improvements are performed on the manufacturing process

1/ The complete manufacturing process has been placed under statistical process control.
The result has been the ability to optimize the balance between different linked parameters :

- the size of the electrode of the resonators has been improved : too large an electrode causes an increase of spurious. But when it is too small it increases iterative impedance and consequently it makes the filters more sensitive to the coil performance. The exact compromise has been defined. As a consequence, in order to insure the reproducibility of this results we had to defined a new and more precise tooling manufacturing technology.

- the manufacturing complexity has been differently split between resonators and filter : in order to achieve a good filter, the 4 resonators need to have a small differential value of impedance and complementary spurious responses. In order to allow relaxed absolute tolerancies on resonators a grouping algorithm has been developped to define assembly kits leading to a good filter.

- to get the mass of information needed by SPC and to insure its quality, new automatic measuring equipments have been developped for resonator characterization. The most critical parameters -inductance and spurious- are now measured in line with a high level of accurary (3 % on inductance value).

2/ The manufacturing of the piezoelectric plates has been put under automatic lapping control. This technology has demonstrated a high level of reproducibility suitable for further ion etching. The consequence will be a reduction of operating costs. Figure 3 Shows the evolution of the frequency versus time for a batch of plates at the beginning of lapping (left). the spread of absolute thickness is reported on the right. One can notice the gathering of the thickness values.

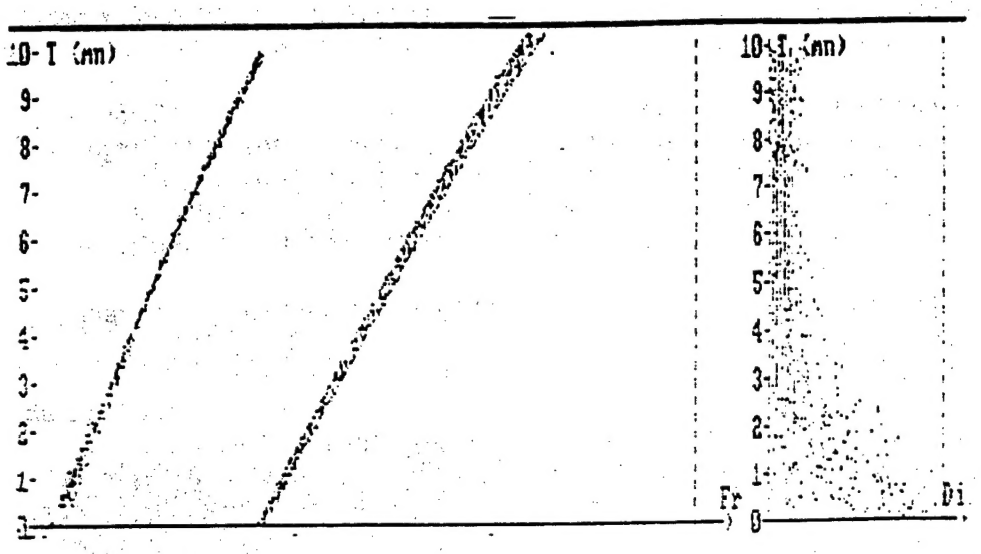


Fig 3.
Automatic lapping control : beginning of the batch treatment and progressive reduction of thickness spread

3/ Ion etching is a main factor of cost for the plates. Drastic improvements are being performed in order to increase the diameter of homogenous etching and consequently, to increase the number of plates per batch. To face the increase of production new equipments have been purchased.
Aside, an automatic machine has been developped to place the glue, the plates and its individual mask on the etching site.

4/ Processing of resonators is the major factor of cost in the filter. It would be very interesting to make 2 resonant functions on the same plate. Works are performed towards this aim. The main difficulties come from :

- the available space on a ion etched plate, which is far smaller than on a lapped plate due to the stiffening ring all around.

- the increase of spurious generation due to the proximity of the 2 resonators.

Figure 4 Shows a typical view of the response of this new kind of filter

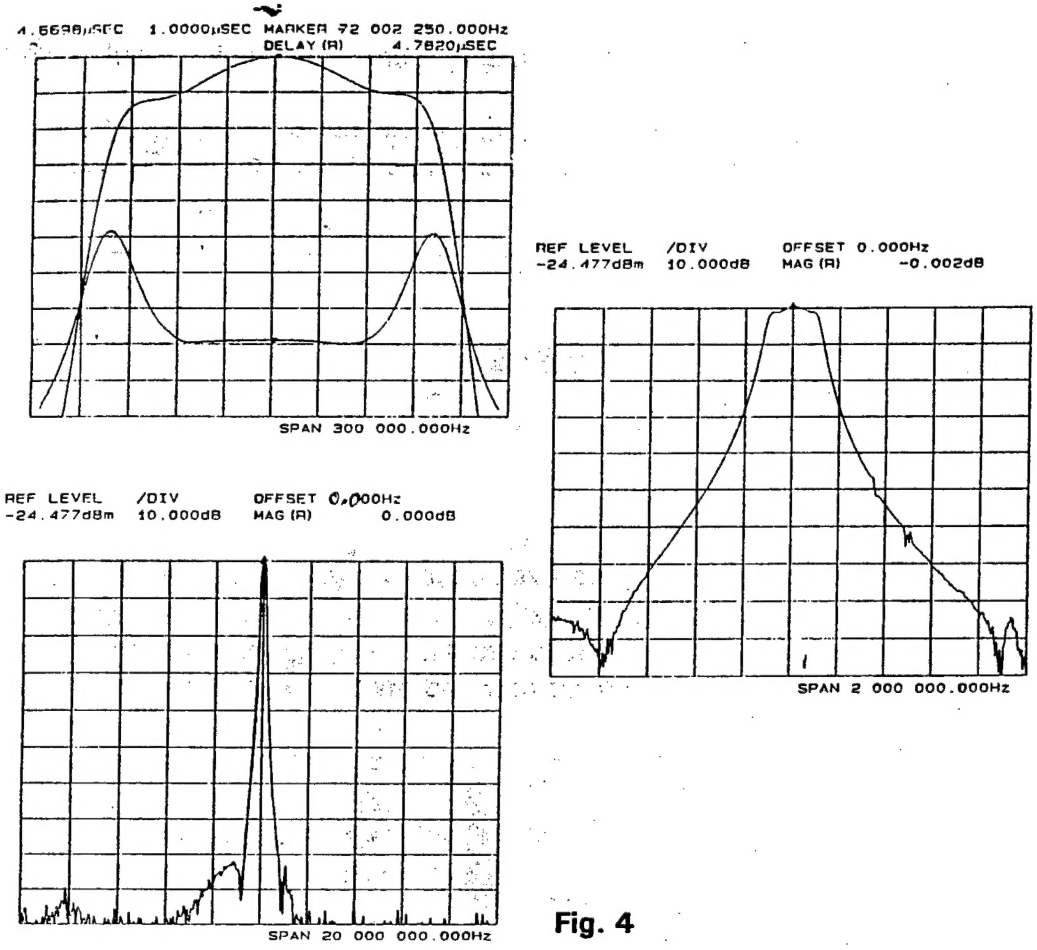


Fig. 4

B/ MOBILE STATION

The filter developped at CEPE has the following characteristics :

- Centre frequency Fc :	45 MHz
- Shape :	4 poles
- 3 dB bandwidth :	200 kHz min
- Stopband rejection :	18 dB min out of Fc ± 200 kHz
	45 dB min out of Fc ± 400 kHz
- Out of band rejection :	60 dB min
- Insertion loss :	6 dB max
- Group delay ripple :	500 ns max over 70 % of the 3 dB bandwidth
- Spurious rejection :	40 dB min
- Input level :	0 dBm
- Temperature range :	-20 , +70°C
- Package :	4 pins DIL 14
- Dimensions :	20 x 13 x 5 mm (see fig. 2 - left)

The electrical design has been fully driven towards the aim of low cost and suitability to mass production.

The technical choices have been defined according to the following :

- number of poles has been limited to 4. A bigger amount of poles would lead to excessive tuning complexity. In order to achieve the suitable performance in stiffness and group delay flatness, a specific synthesis algorithm has been developped and implemented on a CAD working station. Figure 5 Shows the typical predicted sensibility of the filter

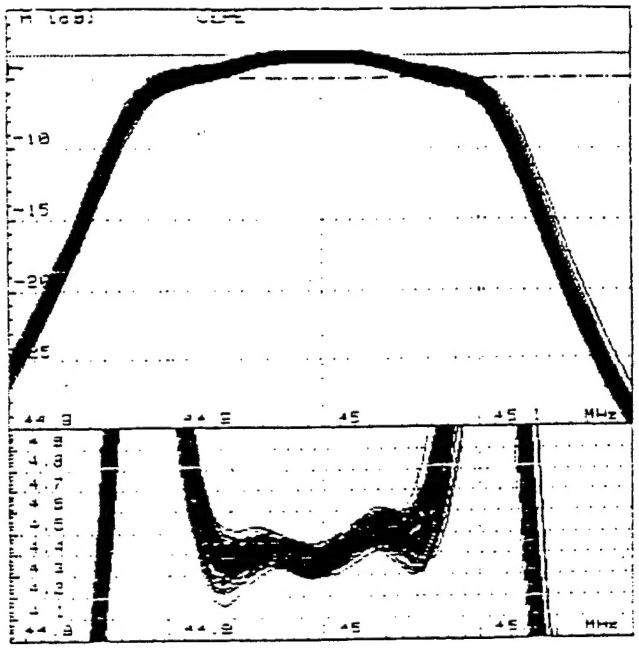


Fig. 5
Sensibility study on the mobile filter

- the 4 resonators are placed on the same plate in order to get the minimum material and processing costs, in addition with minimum size. And, in order to ease the tuning of the filter, the mechanical coupling of the resonators has been excluded.

- we need to use a high coupling piezoelectric material, in order to reduce the spurious generation due to the proximity of the resonators. Lithium tantalate has been chosen.

- we had to avoid ionic etching. Among the frequencies interesting the system, 45 MHz was suitable for that aim (45 MHz is made on a 45 μm thick plate. This thickness is achievable by lapping). Fortunately the relative bandwidth of the filter calculated with 45 MHz agrees with the use of lithium tantalate.

- the electrical scheme of the filter had to be very simple and as far as possible had to avoid coils. Finally, there is only one coil, and its very low quality factor requirement is consistent with the use of a chip.

- internal assembly should be surface mounted in order to minimize size.

This was the basis of a new filter concept. The industrial implementation required to first overcome various feasibility points either on the product and on the manufacturing process, and then to optimize them.

1/ Mounting the plate :

The plate is mounted flat on the printed alumina substrate.

Due to the electrical scheme, 8 electrical connexions are needed. This is cause of a strong assembly, but, in fact, too strong an assembly is disadvantageous because of the strains induced on the plate. The consequences may be an increased shift of frequency versus temperature, or even the break of the plate.

Numerous experimentations have been performed to define the right nature of glue and curing and the right disposal of fixing points. The need for automatic mounting of the plate has also been taken into account. The result is a temperature shift quite conform to the free plate theoretical behaviour.

2/ Unwanted coupling :

The proximity of resonators on the same plate may cause spurious responses even on lithium tantalate.

On the contrary increased proximity reduces the spread of characteristics between the resonators : it increases the ease of tuning and diminishes the size of the plate and consequently the cost.

Numerous disposals of the resonators have been tested to reach the right compromize

3/ Tuning :

For classical filters, tuning is performed by adjusting or exchanging the coupling components. The very compact design of the mobile filter makes it impossible to achieve such an operation. In addition it is a quite cost consuming step of fabrication. This operation has been suppressed and replaced by a prediction of the exact values of the components needed. A special algorithm has been developped to calculate these values from the measurements of the whole set of resonators, including the tolerances of the components.

It has required the design of a performant measuring head to pick information directly on the very small size filter without generating electrical distortions.

4/ Prototype line

A prototype manufacturing line has been implemented. It encompasses newly developped fully computer assisted equipments such as :

- plate mounting
- coupling components prediction
- placing components

It has a capacity of 10.000 filters per year, and has yet produced 1.000 filters. A full capacity line may be implemented in a short delay.

The mobile IF filter that CEPE has developped is approximatly 3 times smaller than a classical equivalent bulk filter. Even compared with other technologies such as saw filters, it has reached an unequaled small size regarding its electrical performances. But we know that the need will be in the future for an even smaller size, especially with the increase of hand held mobile telephone. That is why works are under progress to achieve an extra factor 2 reduction on size, so that the overall dimensions will be 13 x 13 x 5 mm (4 pins DIL 8 package). Figure 5 Shows the first results on electrical response

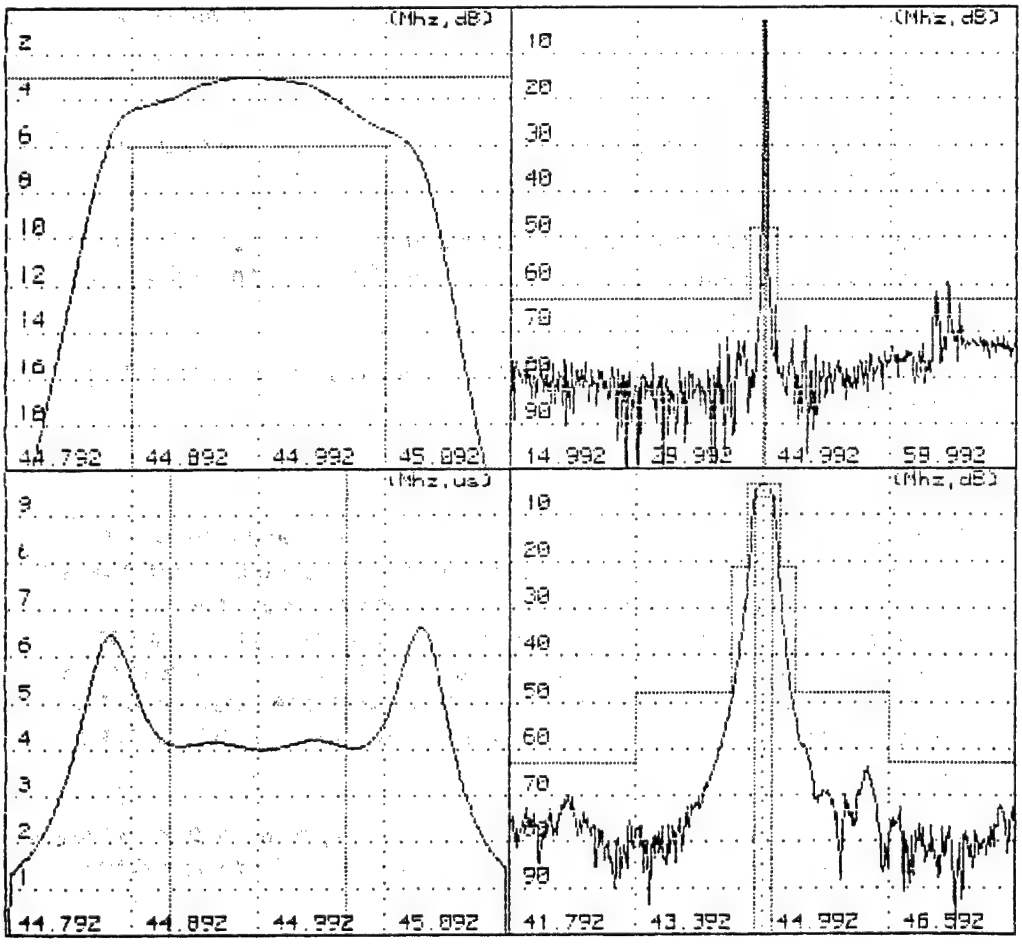


Fig. 6

Electrical response of a DIL 8 package mobile filter

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Real - Time ASIC Implementation of a 4.8 Kbit/sec CELP coder

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ABSTRACT

This paper describes the design and VLSI implementation of a system that achieves vocal compression at 4.8 kbit/sec employing Code-Excited Linear Prediction (CELP) technique, selected as the U.S. D.o.D. standard for a 4800 bps voice coder.
A microprogrammable specialized architecture based on fixed-point arithmetic and a 512 vectors codebook has been developed and. using extensive pipelining with addressing, data reading, calculating and writing cycles performed in parallel in one instruction time-slot, we achieve a peak performance of 20 MIPS with very low overhead. at a 40 MHz clock frequency.
The chip directly interfaces external DRAMs to store coded speech; it can be used for channel coding and solid state recording applications. The chip is being implemented in a 1.0 µm double-layer metal CMOS process.

I) - INTRODUCTION.

High quality. low bit rate (below 9600 bit/s) speech coding is one of the most interesting research fields whose advances pave the way to manifold applications: mobile telephone systems, data and voice integrated networks, voice-recording systems.
Code Excited Linear Prediction (CELP) was introduced in 1984 [Atal.1984] as a coding technique able to achieve high quality speech at medium and low bit rates. CELP coding is based on linear predictive analysis to model the speech spectrum short-term formant structure, and on analysis-by-synthesis search procedures to determine perceptually optimized excitation signal and long-term spectrum periodicity.
The closed loop search can be described as a two stage vector quantization (VQ) procedure: an adaptive code book models the long-term signal periodicity, while a fixed stochastic code book is used to model the residual from short-term and long-term prediction.
Computational requirements of the overall algorithm depend essentially on adaptive and stochastic code book sizes; these affect also the quality of the resynthesized speech signal. Real-time CELP implementation requires a significant effort to reduce the complexity of the original algorithm without loosing performance.
Our approach follows coder structure, bit allocation and computational shortcuts adopted in the standard proposed by the U.S. Department of Defense (PFS 1016)

[Kemp,1989][Campbell,1989]; the main difference being that we achieved a comparable quality with a fixed point arithmetic [Flaiani,1990].
Table 1 shows computational requirements of CELP implementation at different levels of coder complexity; we have assumed that LP analysis and adaptive code book search consumes approximately 4.3 MIPS.

Code Book Size	Stochastic Search	Total MIPS	DSP Chip Rating
128	2.1 MIPS	6.5 MIPS	13 MIPS
256	4.2 MIPS	8.5 MIPS	17 MIPS
512	8.3 MIPS	12.6 MIPS	25 MIPS

Table 1. CELP Computational Requirements.

These MIPS values refer only to multiply, add, multiply-accumulate, compare and divide and should not be confused with DSP chip peak ratings; programming overhead and pipeline's breaks lead to floating point DSP rating of about twice the algorithm complexity [Campbell,1990] .
For this reason real-time implementations using commercially available DSP must reduce the codebook size decreasing synthetic speech quality [Casajús,1990] .

II) - THE CELP ALGORITHM.

CELP analysis consists of three basic functions: short delay "spectrum" analysis; long delay "pitch" search; residual "code book" search.
Short delay spectrum analysis is estimated, on a 30 ms Hamming windowed frame size, by 10th order autocorrelation LPC analysis. Sample rate is 8 KHz.
Long delay pitch search and residual code book search are performed on a 7.5 ms subframe, four times per frame.
The adaptive codebook is 256 codewords wide: it contains 128 integer delays and 128 non integer delays (fig. 1); the pitch delay is delta searched, relative to the previous pitch, for every even subframe.

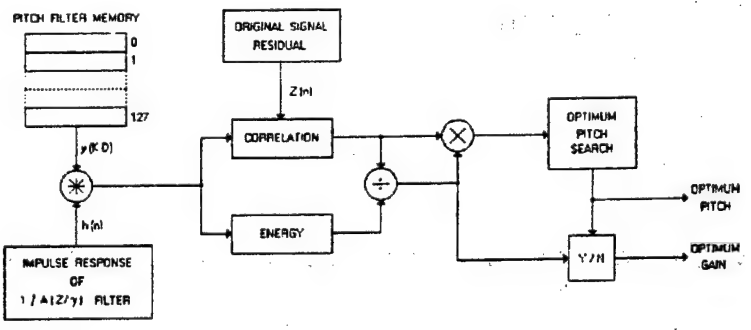

Fig. 1

The stochastic codebook size is 512 codewords (fig. 2): codewords are pseudorandomly generated, ternary valued, overlapped, and approximately 75% sparsed (zero values); these design choices allow to implement efficient search procedures [Lin,1987].

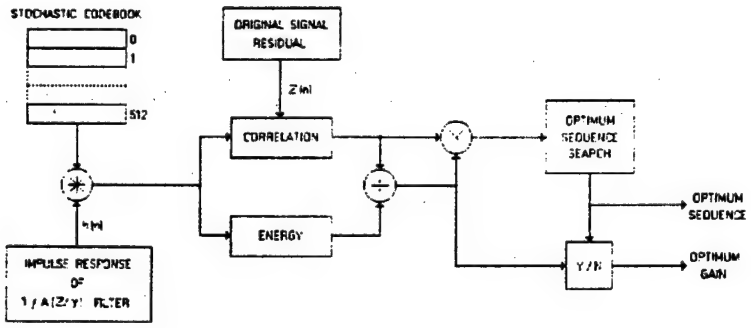

Fig. 2

The indexes of the adaptive and stochastic codebooks, and the gains associated to the optimum codewords, are computed according to a minimum squared prediction error criterion including a perceptually weighting function that improves subjective speech quality by exploiting masking properties of human hearing.
CELP synthesis consists of the same three functions (performed in reverse order), plus a fourth function, called "postfiltering", (fig. 3) to enhance the synthetic output speech [Chen,1987].

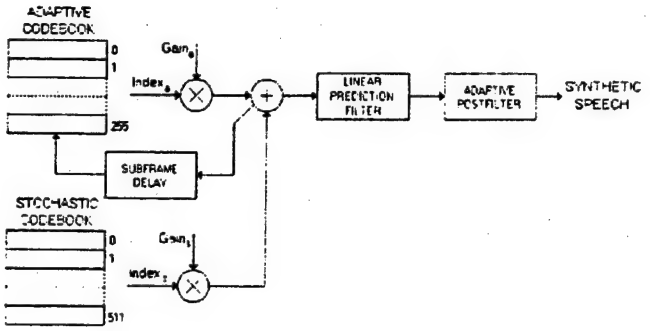

Fig. 3

Table 2 shows the quantization scheme adopted for our CELP algorithm.

	Spectrum	Adaptive Codebook	Stochastic Codebook
Bits per Frame	34	index: 8+6+8+6 gain: 5x4	index: 9x4 gain: 5x4
Rate	1133.33	1600	1866.67

NOTE: the remaining 200 bps are used as follows: 1 bit per frame for syncronization, 4 bits per frame for forward error correction, 1 bit per frame for future extensions.

Table 2. CELP bit allocation scheme.

III) - CHOICE OF THE INTERNAL WORDLENGHT.

A fixed point VLSI implementation of the CELP coder raises the issue of the internal wordlenght width; this must be chosen as a compromise between the requested accuracy and the silicon area occupied. Also, this internal wordlenght may be different in different parts of the processor (for instance, the accumulator has always extra bits to avoid early overflow). From the point of view of wordlenght choice, the linear prediction is the most critical computation of the whole algorithm. This fact stems from the particular kind of calculations involved, requiring the division of quantities obtained by accumulation. Since in the proposed architecture all the calculations are performed by the same arithmetic unit, the wordlenght choice for this unit must be set up on the severest condition.
Extensive comparisons between prediction coefficients computed in floating point and fixed point arithmetic with various wordlenghts have been carried out in order to define the minimal requirement. The results can be summarized as follows.
If the wordlenght is below ten bits, the linear prediction algorithm cannot converge to a significative result. Increasing it over ten bits, significative prediction coefficients are obtained, with differences from the reference ones (floating point) decreasing with increasing wordlenght. Taking into account the ensuing manipulations (LSP encoding and coarse quantization) the additional accuracy obtained with wordlenghts over 16 bits becomes negligible. For this reason a wordlenght of 16 bit has been chosen. To obtain the best results, some intermediate operations have been customized in a suitable manner: for example we have introduced rounding after multiplication and ordered some arithmetic operations in a suitable sequence.

Similar tests have been carried out on the two stage V.Q. procedure. In order to decouple the effects of the linear predictive part of the algorithm, initially the two analysis by synthesis procedures were tested (with wordlenghts of 8,12 and 16 bits) using the "reference" spectral coefficients computed in floating point.
The final result was that 8 bit are sufficient to obtain an intelligible, though distorted, synthetic speech; with 12 bit results are fairly good; with 16 bit the quality is nearly indistinguishable from that obtained in floating point.
When the algorithm is all implemented with the chosen 16 bit wordlenght there is a very little degradation of the overall quality, nearly totally accountable to the linear prediction block.

IV) - SYSTEM ARCHITECTURE.

System architecture is depicted in figure 4.

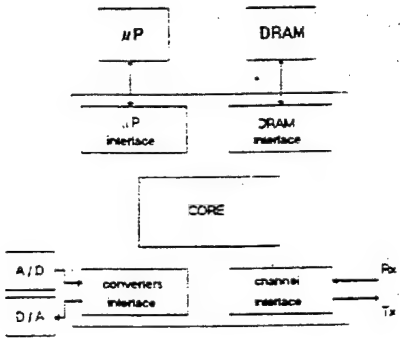

Fig. 4

The system is controlled by a microprocessor that sends commands, data and parameters and read back data and status information through a host interface, organized around a 4 bit address bus, an 8 bit data bus and three dedicated signals (WRITE, DATA STROBE, READY).
Commands are stored in the COMMAND REGISTER, connected to the CORE through a decoder; a bidirectional register (M/S) holds flags with current mode and status information: 3 ADDRESS REGISTER are used as pointers to internal or external memory; and four DATA REGISTERS are used for data transfers.

The DRAM interface is made up of a 4 bit data bus, 11 bit multiplexed address bus, 7 control signals (RAS0-3, CAS, WE, OE); up to 16Mbits of external memory can be connected using four 1Mbitx4 chips or one 4Mbitx4 chip, allowing about 60 minutes of coded speech to be recorded. Bandwith requirements are very loose, so special modes for fast access (fast page mode, interleaved mode, nibble access mode) are not implemented.
To ensure a correct REFRESH cycle, the interface generates a "continuous" CAS BEFORE RAS signal that can be interrupted by a read or write request; in this case the DRAM interface changes controls signal in order to ensure the correct read or write operation.

Figure 5 depicts read operation timings.

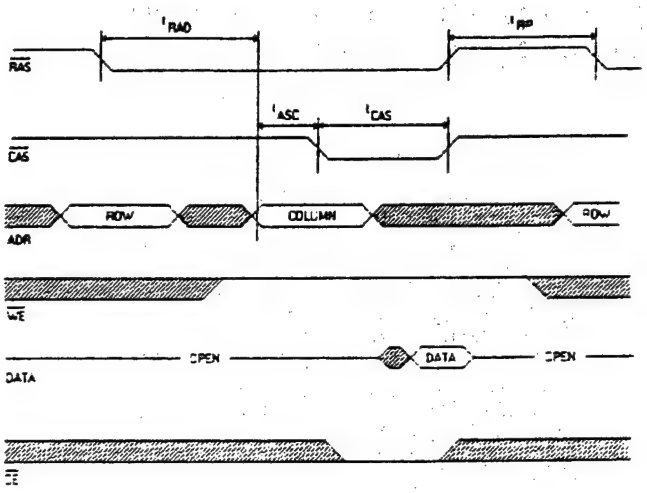

Fig. 5

If tRAD = 50 ns, tASC = 50 ns, tCAS = 100 ns and tRP = 200 ns, we have a cycle time of 400 ns.
DRAM and host interface are tightly connected in order to allow a fast access from the microprocessor to the external memory.

The channel interface provides four dedicated pins: SERIAL DATA IN, SERIAL DATA OUT, CLOCK_A and SYNC_A. The converters interface follows the standard serial protocol of combos and Σ/Δ devices, providing three dedicated pins: SERIAL DATA I/O, CLOCK_B, SYNC_B.

The CORE can be divided into four blocks, as depicted in figure 6: Chip Control Unit, ALU, MEMORIES and I/O.

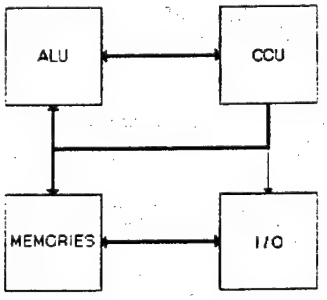

Fig. 6

The CCU (fig. 7) performs instruction fetch, instruction decoding, hardware loop control, branches and subroutine calls control.

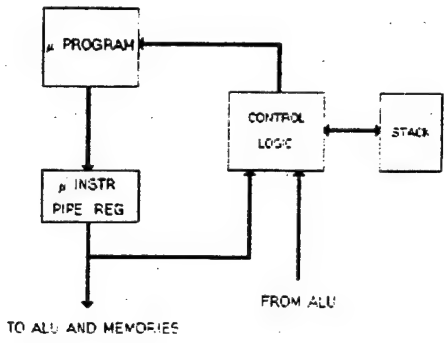

Fig. 7

Referring to figure 7, a new instruction is read from memory every 50 ns, and after 25 ns the instruction is stored in the PIPE REGISTER; at the same time the new microprogram address is latched in the MICROPROGRAM COUNTER register; in the next 25 ns it is possible to change this address, in case of microinstructions that modify the microprogram flow.
The CONTROL LOGIC block contains counters and registers used to perform instructions loops and nested loops with very low overhead, while the STACK is a separate internal memory that stores the contents of several registers in case of nested loops, branches and subroutine calls.

The ALU block of figure 6 is a fixed point arithmetic unit that contains a 16x16 bit multiplier, a 22 bit adder/subtractor, a 32 bit barrell shifter and a set of dedicated and general purpose registers .

The MEMORIES block of figure 6 contains an ADDRESS GENERATOR UNIT; in order to optimally exploit the ALU we generate, in a 50 ns time slot, two new read addresses and one new write address with the timings depicted in figure 8, that also shows the pipeline of the ALU and ADDRESS GENERATOR UNIT operations.

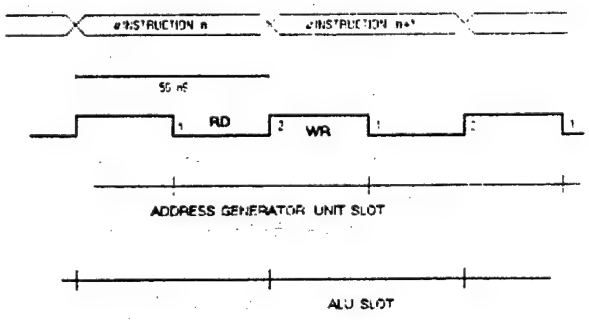

Fig. 8

1) latch NEW ADDRESSES for READ
1-2) READ RAMS
2) latch DATA for new ALU operations and RESULTS for WRITE
2-1) WRITE

1-1) NEW ADDRESSES GENERATION
2-2) ALU OPERATIONS

The I/O block of figure 8 contains two RAMs used as buffers for temporary storage of speech samples : the input RAM contains one speech frame during LPC analysis, while the output RAM must store only one subframe .

Highlights of the architecture.

The core architecture has been designed for use in a numerically intensive application: three data busses and three address busses link the ALU block with the MEMORIES block in order to read in parallel two RAMs and write a result of a previous elaboration into a third one in a single time-slot. The CCU block features two more internal busses, a program data bus and a program address bus, while there are two different address generation units, one for the internal memories and one for the external dynamic memory.

Moreover, the core architecture differs from most commercial DSPs in loop control. Inside the CCU there is dedicated hardware to control software structures such as loops and "nested" loops with control indexes function of outer loops variables; this highly reduces program overhead and improves equivalent chip rating.

The ADDRESS GENERATOR UNIT for internal memories contains two dedicated arithmetic units, separate from ALU, one with an 8 bits parallelism dedicated to address generation for RAM READ operations and the other with a 9 bits parallelism for RAMs WRITE and ROM READ operations. In a 50 ns time slot each old address can be automaticly incremented or decremented, generating the new addresses.
Data management is simplified and optimized taking advantage of the structure of the algorithm and of the fact that only memories of reasonable size are needed: five different RAMs are used for data and parameters, each with a maximum deep of 240 words.
Also, the core automatically handles modulo arithmetic for efficient circolar buffers management.
Fig. 9 shows the timings of a generic instruction loop, i.e. a(n)xb(n)-->c(n):

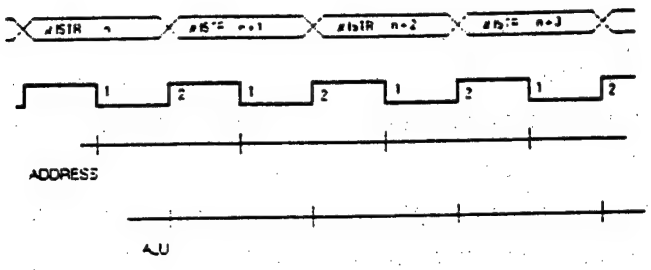

Fig. 9

1) latch NEW ADR
1-2) READ
2) latch DATA in ALU REGISTERS
2-1) WRITE result in RAM
1-1) new ADR generation
2-2) ALU elaboration

V) - CONCLUSIONS.

A flexible VLSI architecture has been shown, allowing the efficient implementation of a CELP coder providing high speech quality at 4800 bits/s.
The chip can find applications in mobile and rural telephony, secure and personal communications, Mobile Satellite (MSAT) and International Maritime Satellite (INMARSAT) Communications; its built-in DRAM interface makes it suitable for low-cost solid state recording.
Future work will be devoted to the task of integrating external A/D and D/A converters in a single chip.

ACKNOLEDGEMENT.

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Microelectronics - Key to advanced system solutions in digital communications

L. Lerach

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Driven by the need for improved communication in todays society, the field of telecommunication has experented a deep-going technologient breakthrough with significant consequences over the past two decades. The latest and most dynamic sector is undoubtedly wireless communication using both analogue and innovative digital transmission techniques. The technical and economic foundation for advanced communication technologies was basically laid by the tremendous advances achieved in the field of microelectronics. Due to the challenging requirements concerning functional complexity, power consumption, compact equipment design and low cost at high volume production, in the field of mobile communications, microelectronics will more than ever play a decisive factor in the further development and the competitiveness of equipment manufacturers products.

To achieve the necessary outstanding innovations in system- and terminal-design with fast response to market needs, different design methodologies are appropriate. While first prototype and low volume solutions are mostly realized based upon available standard components, gate arrays or cell-library solutions developed by the system houses, for high volume applications, under extreme cost pressure and stringent performance requirements, highly optimized dedicated IC solutions realized in close cooperation between system experts and IC manufacturers are most effective. This type of two phase procedure we see being used for GSM terminals presently.

To enter successfully into the market for complex microsolutions for future wireless communication products semiconductor suppliers have to show major success factors such as close system relations, availability of system specific VLSI macros and circuit expertise, powerful CAD tools and appropriate state of the art process technologies and fabrication facilities. Furthermore application and marketing expertise locally available at the customer base is necessary for supporting the IC-user to take advantage of these complex devices.

The combination of high frequency circuitries in the frequency range of up to 1.8 GHz, together with the need for extremely complex digital signal-processing and control as well as speech processing with low band width, results in specific technology demands and will in the long term influence process development and IC-packaging strategies. State of the art technologies used are 1.5 micron oxide isolated bipolar processes achieving a transit frequency in the range up to 10 GHz for RF circuitries and 1 micron CMOS technologies with high packing density, low power consumption and suitability for mixed analog and digital circuits for the audio and DSP part.

Reduction of System chip count and power consumption, incorporation of further functions such as speaker recognition, and RF performance improvements will be possible in future based on the introduction of submicron bipolar, BICMOS and CMOS process generations.

Besides advances in process technology and fabrication techniques, the decisive factors for system innovation will be the skilfull implementation of system and algorithm know how, and the mastery of component complexity with factors 10 to 100 times greater than presently available. To make this possible, close partnership between system, CAD and semiconductor experts is an important ingredient.

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"COPPER ON CERAMIC" CIRCUIT BOARDS FOR HIGH FREQUENCY APPLICATIONS

Dr. D. Jaculi, H. Gernoth, HOECHST AG, Frankfurt am Main, Germany

1. Introduction

Advanced integrated circuit technologies require new solutions for connecting IC-chips with their environment: miniaturization is the key word for designing the so-called "printed" circuit boards. Increasing integration density leads to increasing heat evolution, so that modern base materials must possess high thermal capacities (Fig. 1). Ceramics, e.g. alumina substrates, fulfil these requirements.

On the other hand, mobile communication systems demand electronic devices which are extremely reliable even in the high frequency area. Therefore, copper on ceramic circuit boards (CCC-boards) offer a good alternative in the low-cost/high-tech field of electronic devices (Fig. 1).

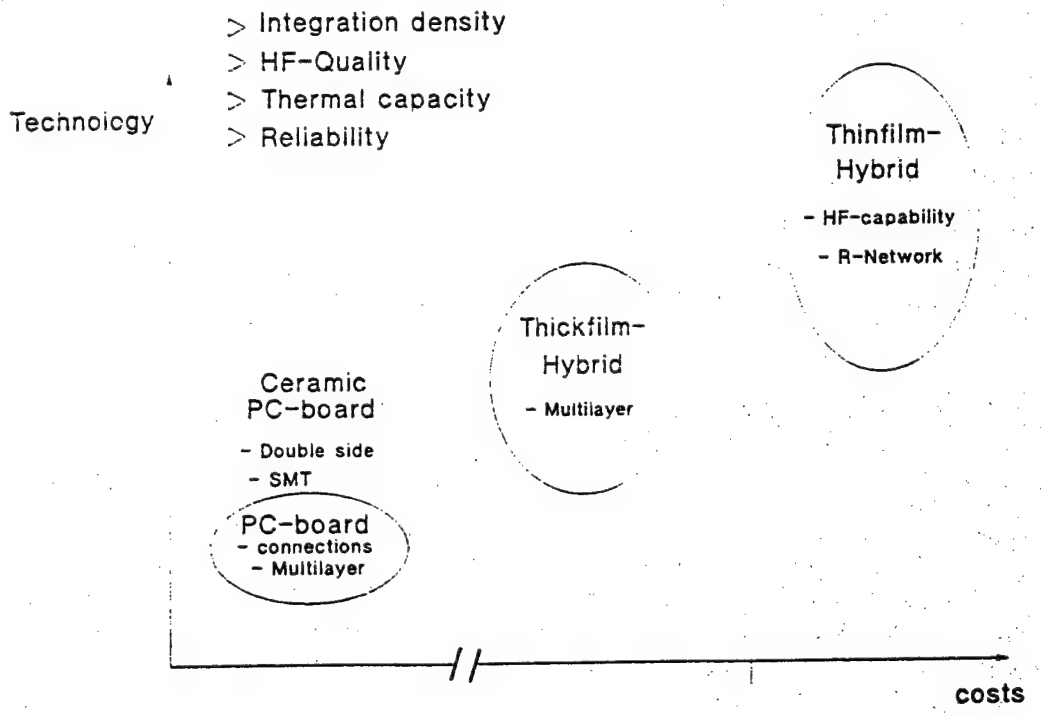

Fig. 1

2. Copper on Ceramic Process

To cover alumina substrates with pure copper, we favour the following process steps (Fig. 2):

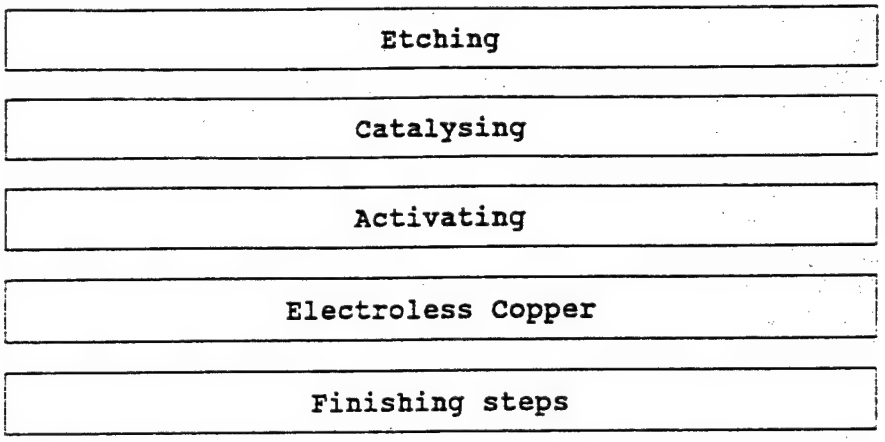

Fig. 2

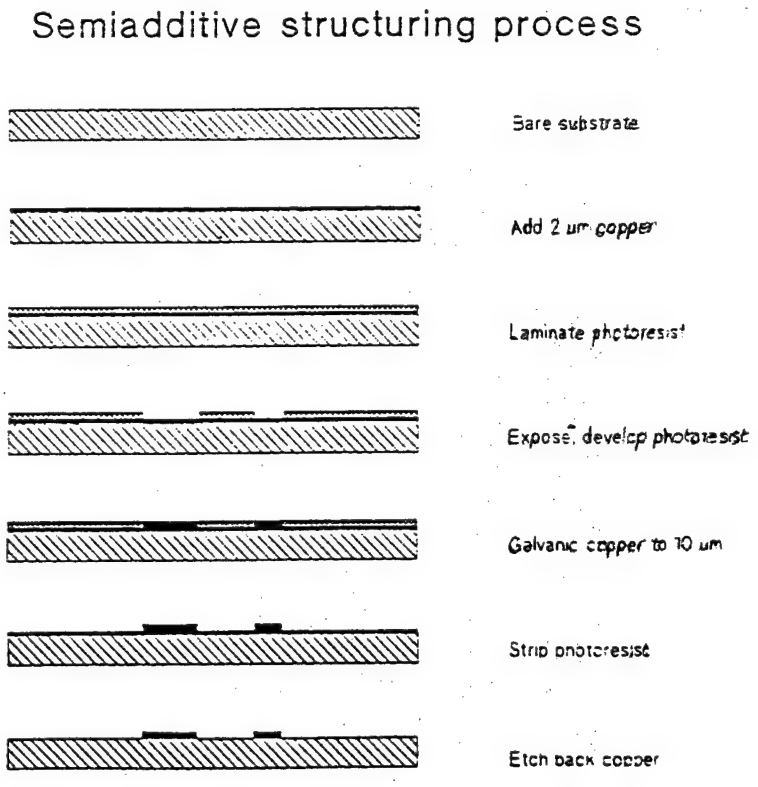

Fig. 3

First, the as-fired surface is roughened in order to enhance the adhesion strength of the deposited copper. We prefer an etching process with strong inorganic acids at elevated temperatures.

Copper deposition follows a modified chemical reduction sequence which is well known in "classical" printed circuit board manufacturing (Fig. 2): the substrates are pretreated by dipping them into a bath of palladium-tin colloids and activating them by an acid solution. The thus prepared catalytic centres initiate the following chemical reduction of copper. By varying the exposure time in the chemical copper bath, copper layers of thicknesses between 0.1 and 10 microns can be achieved.

Depending on the specific application, either a semiadditive or a subtractive method can be used to build up the circuit lines. For simplicity's sake we show here the semiadditive path (Fig. 3): the photoresist is laminated onto the chemical copper layer, it is imaged and developed, and finally galvanic copper fills the resist trenches up to the desired copper thickness.

3. Properties

3.1. Adhesion Strength

The adhesion force cannot be determined directly. However, two different methods are well established to measure the connecting strength between copper and the alumina substrate: they are called the pull- and peel-test.

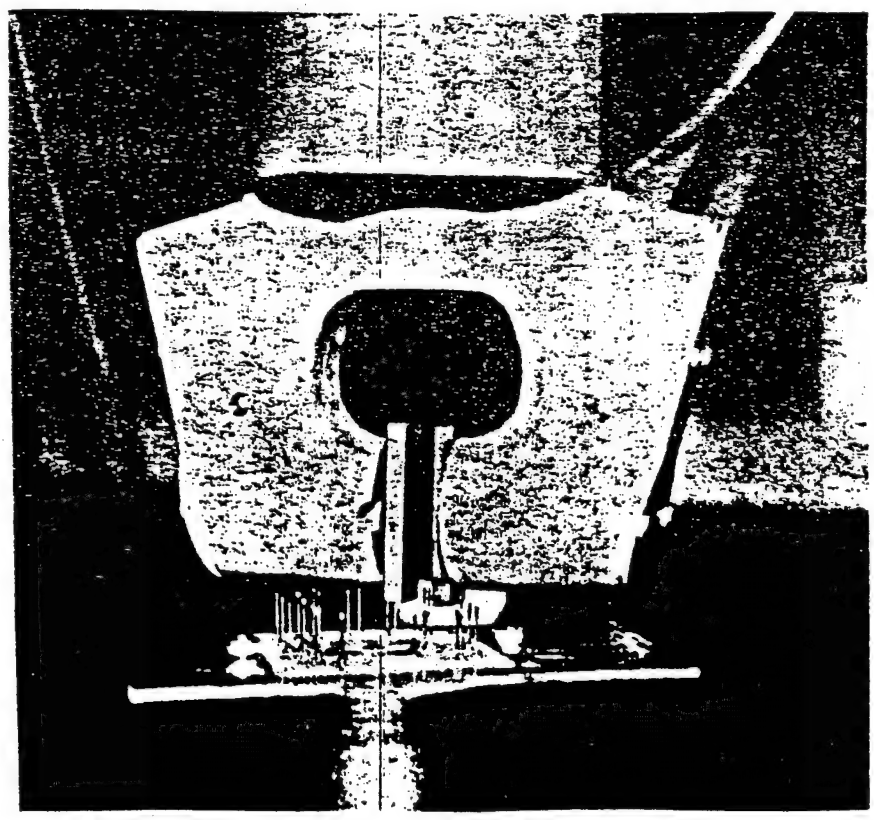

Fig. 4

- For the pull-test small pins are soldered onto the copper layer. The testing-machine (Fig. 4) measures the force to tear these pins off the basic substrate. The resulting force per unit area is called the pull-strength. For CCC-boards, it always exceeds a value of 30 MPa, the pull-strength for epoxy-glues.

- To perform the peeling-test, small strips of copper are torn off at an angle of nearly 90 degrees (Fig. 5). The peeling-value is the ratio of the average peel-force and the torn-off width. For CCC-boards, it is always greater than 0.6 Nmm^{-1}.

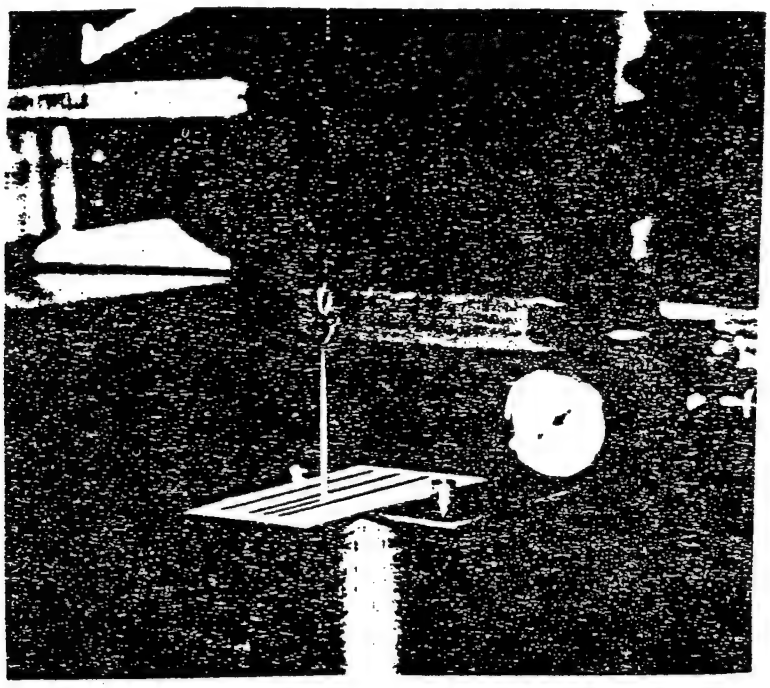

Fig. 5

3.2. Electrical properties

The electrical resistance is a function of the copper thickness. Applying a simple test method, if the layer exceeds about 5 microns, the resistance will decrease to the value of pure copper (Fig. 6).

For high-frequency applications the skin depth (Fig. 7) is a significant parameter. Up to 500 MHz the skin effect takes place in the upper 5 microns of copper. In the GHz-area it falls down below 2 microns.

As a conclusion, for most practical applications a minimum copper thickness of 5 microns seems to be reasonable.

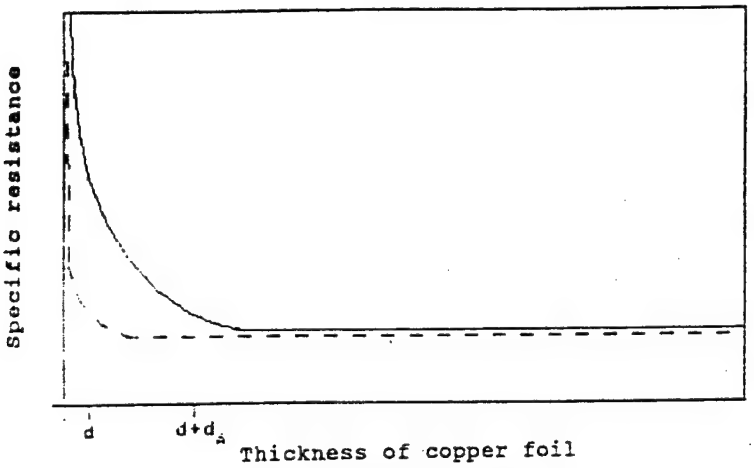

Fig. 6

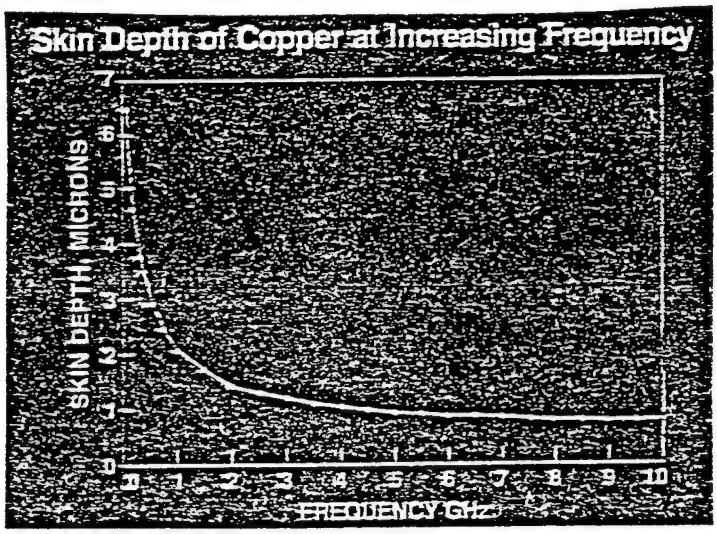

Fig. 7

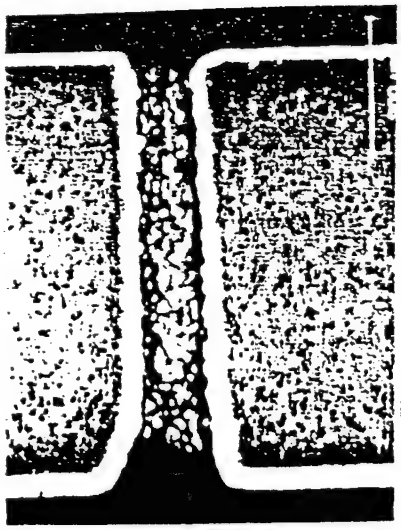

Fig. 8

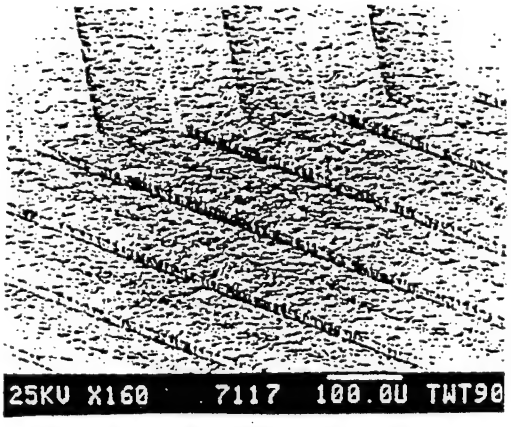

Fig. 9

3.3. Vias and Line-Resolution

Vias are "shot" into the as-fired ceramics by a laser. Through-hole metallization is possible in vias with only 150 microns diameter or greater (Fig. 8).

Photoresist imaging allows to decrease line width and spaces down to 50 microns (Fig. 9). Fine line technology also produces circuit lines with an exact geometry which is essential for high frequency applications.

4. High-Frequency Applications

The properties of a high-frequency amplifier depend on the applied frequency and the geometry of the circuit lines (Fig. 10). The amplification power (Fig. 10: upper curve) remains constant in the lower and medium frequency region. It breaks down only at very high frequencies.

The measured reflexion power is extremely sensitive for geometry failures. As shown (Fig. 10: lower curve) the reflexion losses tend towards a minimum at medium frequencies.

Compared to the same circuit in thick film technology, the CCC-boards show better high frequency properties due to the higher geometrical resolution.

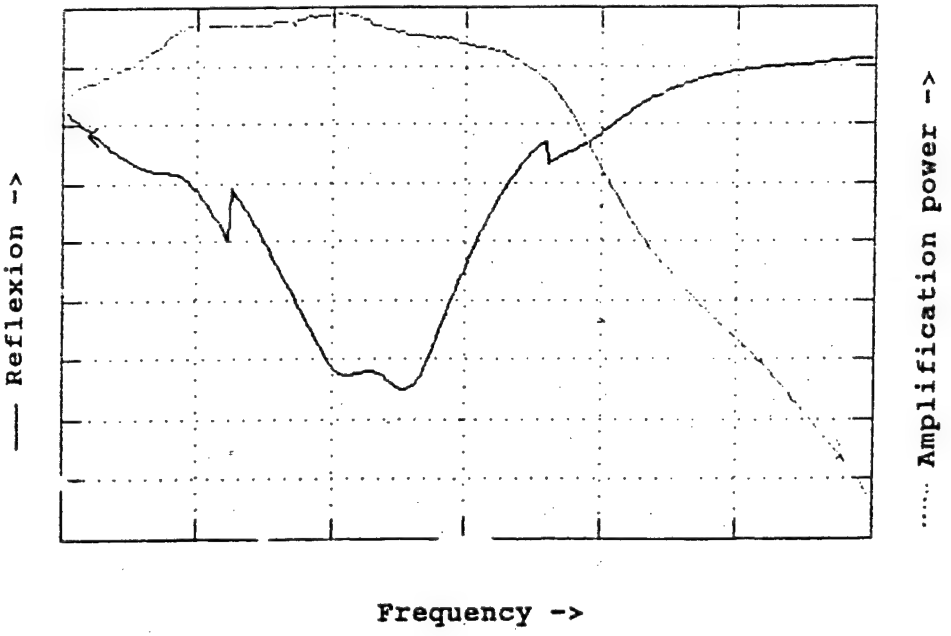

Fig. 10

5. Conclusions

Copper on ceramic circuit boards combine the advantages of ceramic base materials and fine line technology: high thermal conductivity and exact geometry of the circuit lines.

Mobile communication in the future will undoubtedly be dominated by high frequency techniques. An ideal tool for modern communication systems is represented by copper on ceramic circuit boards, which are successfully applied even in the upper GHz-band.

FINISHING OPTIONS FOR FINE PITCH ASSEMBLY

FPTfinish.txt

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1. Introduction

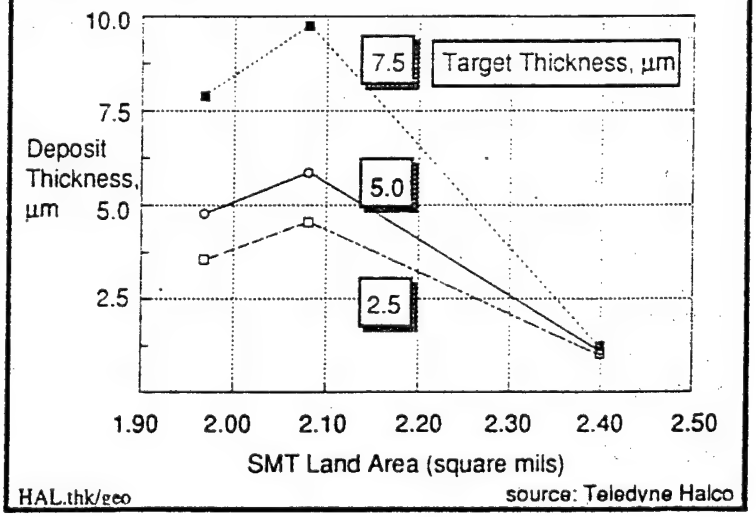
The need to assemble high I/O components packaged both individually and as multichip modules is generating considerable interest and activity at the printed wiring board level. The general perception is that existing solder coating processes based on either hot air leveled or conventional IR reflow will not be capable of providing the uniformity and control needed by the coming generation of fine pitch packages. These are taking a number of forms, but those presenting the most significant challenges at the board and assembly level seem to be the so called SQFP (shrink quad flat package) configurations which are an extension of the EIAJ QFP package family: the EIAJ outline remains constant while lead pitch decreases to reflect the need for higher I/Os, while the JEDEC QFP maintains a standard lead pitch of .025". Therefore at high lead counts, the SQFP package will go to a lead pitch of 0.3mm. Lares has had experience with 320 I/O packages requiring 0.25mm leads on 0.4mm centers, and this report is intended to present some of the impressions resulting from this activity. The objective was to evaluate the capability of various finishes to provide an attachment surface of controlled thickness, considering also the solderability of these finishes in assembly. The termination methods assumed to be required will demand the use of controlled stencil sections, fine particle solder paste, vision recognition and IR reflow in a screen paste/mount/reflow sequence that will provide good results down to approx. 0.5mm lead pitch. Below that, two trends are emerging: the industry will look to the pwb fabricator for a fusible overplate consisting of closely controlled solder deposits on the component pads which will reduce or eliminate the need of the assembler to screen solder paste, or paste/flux systems which represent a significant departure from general practice will be used over a nonfusible finish.

2. Fusible Overplates

2.1 Hot Air Solder Leveling

While the doubts expressed by many users as to the possibilities for control of solder leveling for FPT assembly have been amply justified both in our experience and that of the industry in general, the potential this technology has for improvement and the well-established specification base behind it should not be overlooked. The new generation of horizontal solder leveling equipment has been reported to have the potential for significant improvements in coating thickness uniformity

Fig. 1: Solder Deposit Thickness vs. Pad Dimensions

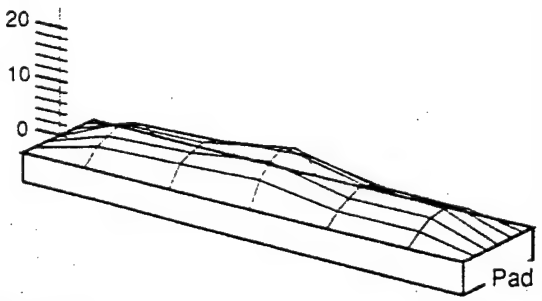


within a given set of pad dimensions[1]. Product literature and user reports indicate these processes can realize a standard deviation of <2 , and while the horizontal technique remains sensitive to the interaction between solder surface tension, airstream impact, and pad dimensions as shown in Fig. 1, productivity and reasonable facility cost will make this option hard to beat for price/performance ratio. FPT patterns in the test series were hot air levelled on a vertical machine (conventional technology). The nominal values seen below do not include areas where solder coverage decreased to less than 1 micron, although these were observed on some of the FPT footprints.

FPT SQFP: Observed mean: 14 Standard Deviation: 4.7

Thickness distribution on pad:

Fig. 2: Deposit Geometry: Hot Air Leveled Finish



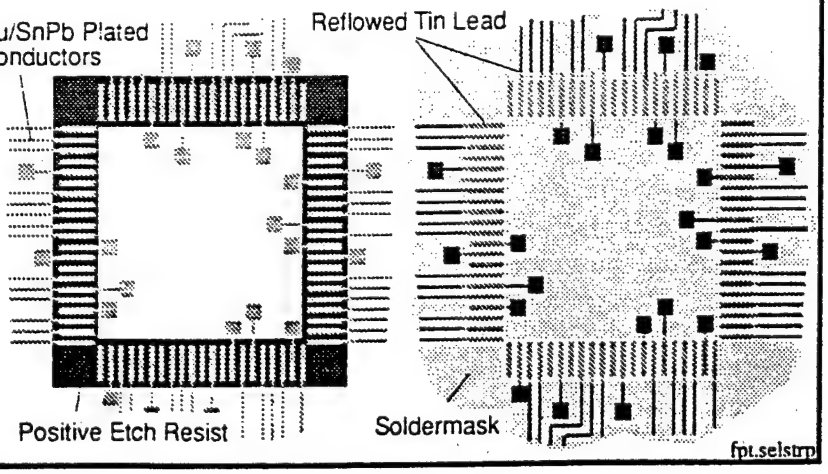
2.2 Reflowed Solder

This option offers the best repeatability of the fusible overplates, but suffers from two disadvantages that are common to both electroplated and electroless finishes:

- topography/maximum thickness is highly dependent on pad dimension due to contact angle/surface tension of solder
- high density patterns should be copper only, requiring two imaging steps (added cost)

While the requirement for a second imaging step is common to all selective finish technologies where the finish is confined to an area that is only a portion of the total metallization exposed by the soldermask, the selective solder stripping required by conventional subtractive processing requires a clearance area around the FPT

Fig. 3: Design Points: Selective Electrodeposited SnPb Finish

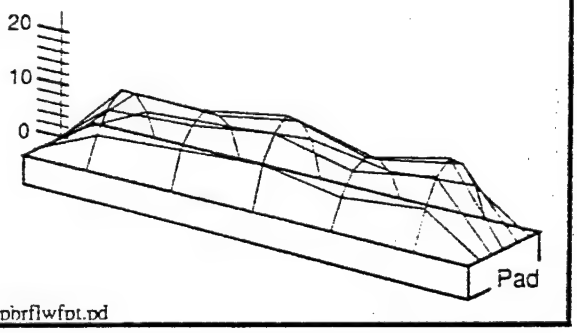


pattern that will permit good encapsulation by the resist used to protect the electrodeposited SnPb during stripping of the rest of the pattern. This will leave "stubs" of fused SnPb under the soldermask, as shown in Fig. 3. While this has not caused any problems in the past, it may take some getting used to for those customers used to seeing the sharp definition of a Hot Air Leveled finish. Another area of concern is that it will be difficult to obtain a thickness of 25-35 : even though the electrodeposited finishes offered the best mix of overplate thickness and uniformity, previous experience has shown that achieving a mean value of 30 of reflowed SnPb pushes a conventional electroplating facility towards economical limits of the process. Typical deposited thicknesses of SnPb used as etch resist or as a conventional reflow finish range from 7 to 15 . A further difficulty has been that achieving this thickness without reducing productivity/increasing cost requires higher current densities which in turn tend to cause an increase in deposit thickness variation.

FPT SQFP: Observed mean: 13.7 Standard Deviation: 2.1

Thickness distribution on pad:

Fig. 4: Deposit Geometry: Reflowed Solder



2.3 Nonreflowed Solder

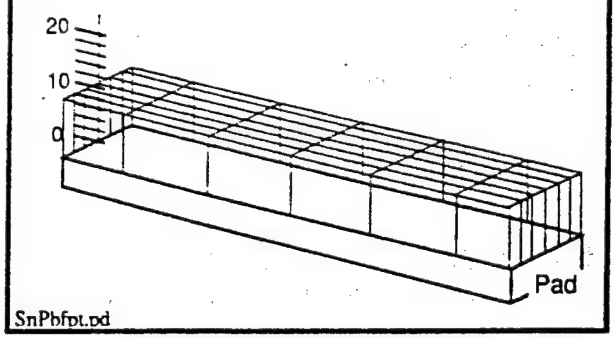
This finish has been considered due primarily to the excellent planarity which can be obtained from a nonreflowed SnPb deposit: the standard deviation was the lowest of all finishes observed except the non-fusible overplates and passivated copper. The unknown here is solderability retention: the lead component in the unreflowed deposit will tend to oxidize over time, requiring agressive fluxes for activation. Available solder volume is a further consideration: being an electrodeposit, this finish has the same thickness limits as noted in (2.2). However, it offers the potential for an impressive level of control as suggested by the observed results:

Mean: 11.2

Standard Deviation: 0.9

Thickness distribution on pad: Fig. 5.

Fig. 5: Electrodeposited Solder Geometry



2.4 Screen Solder Paste (pwb fabricator)

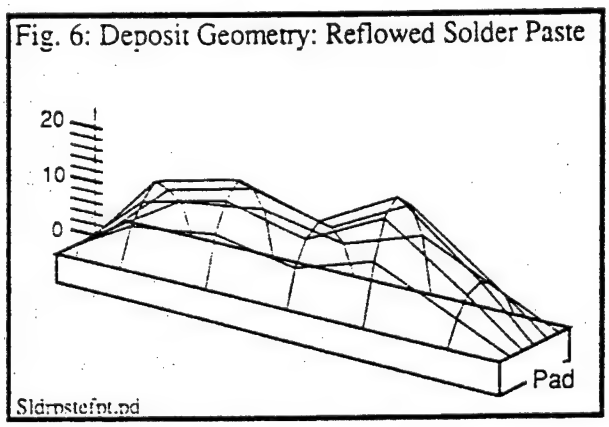
This approach has so far given the best results with regard to total thickness, although the process window is very

narrow. The need to use materials and manufacturing processes compatible with large (500 x 600mm) panel sizes reduces the degree of freedom normally available to this technique in an assembly operation, and the line between excessive numbers of pits in the reflowed deposit and shorts is very fine. The incidence of shorts between FPT pads on 0.4mm centers suggests that the maximum thickness possible using a "window" (nonregistered) definition suitable for large area printing is approx. 25 . As is evident from the standard deviation, tolerances associated with this approach may require adoption of assembly type single board automated processing by the pwb supplier.

FPT SQFP Test: Observed mean: 23.6 Standard Deviation: 8.3

Thickness distribution on pad:

Fig. 6: Deposit Geometry: Reflowed Solder Paste



Recent developments in paste and process technology introduced at the JPCA in June suggest that the lower limit for solder paste processes may not be reached even at 0.3mm lead pitch. Three key factors are contributing to this evolution:

· stencil materials and construction
screens used for fine pitch assembly are tending towards composite construction (metal stencil supported by "tetlon" fiber or stainless steel mesh), while stencils utilize alloys such as nickel-cobalt which exhibit minimum undercut/irregularities in the etched stencil openings and make extensive use of half-etching for local control of stencil thickness;

· solder paste composition and process
fine particle pastes are being seperated from fluxes, enabling the rheology of the pastes to be controlled based on resolution: flux is applied in a seperate step after paste is screened;

· process control
processes make extensive use of automatic registration systems, microprocessor controlled printing parameters, and automation for process uniformity and control.

Typical results of one of these processes are shown in the following table:

Table 1: Thickness Characteristics of Sony "Super Solder" Process

Technology, mm:	0.5	0.3	Bump
nominal deposit thickness, m:	50	20	5
tolerance (2σ), m:	5	2	1

2.5 Photodefined Solder Deposit

There are two processes under advanced stages of development which utilize either a

permanent dry film soldermask or strippable temporary mask to define the solder deposit. The unique feature of both is the formation of essentially flat topped deposits through application of an in-line "micromolding" technique.

SiPad

Developed by Siemens[2], this process uses a conventional dry film soldermask as the photodefinable resist in the following sequence:

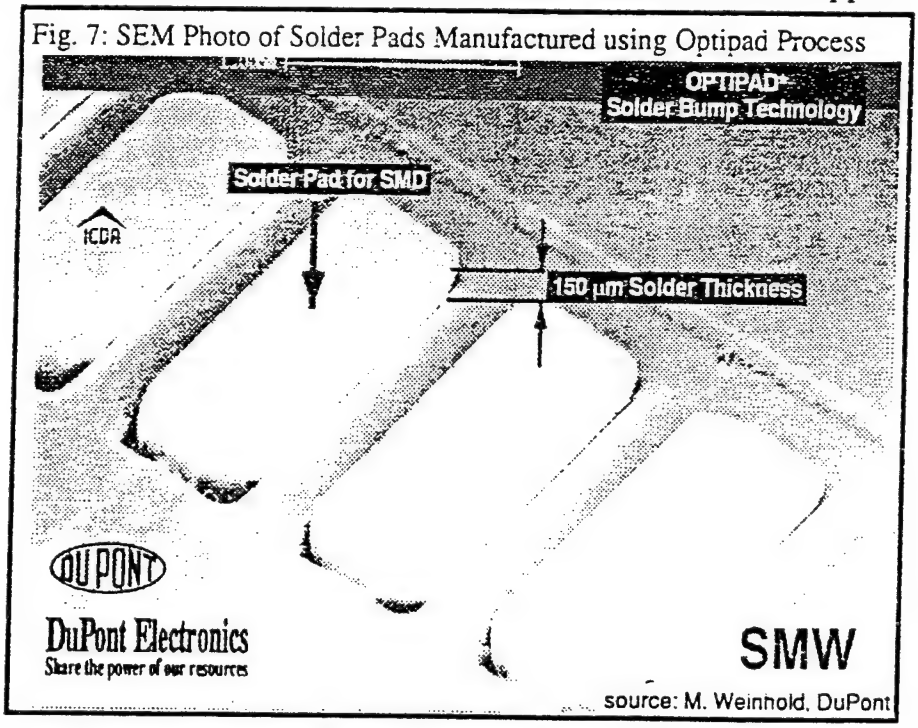
- apply dry film soldermask to pwb
- expose, develop, cure
- screen solder paste in open "pockets"
- reflow paste
- flatten deposit

The result of this process is a solder deposit equivalent in height to the thickness of the dry film soldermask. Solder "dams" (webs imaged between pads) are required, and the process will accept a clearance window around the pads due to the pullback effect of the solder paste.

OptiPad

Invented by Dr. D. Friedrich of SMW[3], this process uses a temporary mask developed by DuPont to define the solder deposit shown in Fig. 7. The mask can be applied over any

Fig. 7: SEM Photo of Solder Pads Manufactured using Optipad Process



solder resist, providing a defined deposit thickness of 50 or 125 m. The process sequence starts with:

- finished pwb, soldermask coated, imaged, and cured
- vacuum laminate Optimask resist
- expose, bake, develop (acqueous)
- UV cure, bake
- solder coat/flatten

· strip resist
· postbake

Optipad offers several process advantages:

+ Complete flexibility of choice regarding soldermask
+ Solder deposit thickness is independent of mask thickness
+ No solder paste printing required
+ Solder coating/flattening is in-line panel process

Disadvantage of both processes will be finished board cost: although the SiPad process does not require the additional photosensitive materials and processing of Optipad it is still necessary to screen solder paste and the resist cost is tied to that of dry film photosoldermask. Clearly an analysis of cost effectiveness of these processes will have to look much more deeply than board cost per unit area.

3. Nonfusible Finishes

The choice here for FPT applications is between nonfusible overplates which maintain solderability (and provide a high level of corrosion protection for exposed metallic surfaces after assembly) and various types of passivation agents and/or prefluxes which protect/enhance copper solderability but have corrosion protection capability after assembly which is highly dependent on end use environment.

3.1 Passivated Copper/Preflux

Passivated copper finishes provide corrosion inhibition of exposed copper either through the formation of nitrogen bearing complexes in the surface of the copper or through the formation of a discrete film on the copper surface. These finishes have been widely used in the Far East for many years, and this finish is also used extensively in Europe by a major US computer manufacturer. It has the significant advantage of presenting a surface which is as flat as the underlying copper foil and electroplate to the assembly operation, and provides solderability retention in controlled storage of 6 months or so depending on flux types used. Some problems have been seen with passivated copper in that the evolution of assembly sequences requiring multiple thermal exposures of various types (IR, Vapor Phase Reflow, Solder Wave) has shown that under certain conditions solderability of passivated copper will not be maintained due to the tendency of the inhibitors to degrade at elevated temperatures. Work to date with no-clean fluxes/pastes suggests that the quality of the solder joint is dependent on the volume of flux within the solder paste deposit available to clean/activate the copper surface: processes which have been developed for use over hot air leveled or other pretinned surfaces tend to give problematic results over passivated copper which has already been through a reflow cycle. The most common form of defect are nonwetted areas on the pad and inadequate fillet formation: both suggest that there isn't enough paste and flux available to do the job. Another alternative, "Mecbrite 4000", is a combined inhibitor-preflux process developed by MEC of Japan and Sony to overcome this problem of solderability degradation through multiple thermal exposures. This process is enjoying rapid growth in the Japanese market and is becoming available in Europe. Compatibility of the preflux with no-clean processing needs to be verified based on end use application.

3.2 Nickel-Gold

- Solderability

When used as a solderable finish thicknesses are nominally 5 of Nickel and 0.1-0.5 of usually "hard" or cobalt gold, 99.9% pure, hardness 160 V.P.N. Gold thickness is kept to a minimum to avoid excessive contamination of the SnPb alloy through intermetallic formation. Due to the highly soluble nature of gold in tin, the wetting characteristics and solderability of a gold finish are excellent and will not degrade over time provided that the gold is neither contaminated nor permits oxidation of the underlying nickel. In effect, the solder joint is formed between nickel and the SnPb alloy, while the gold goes completely into solution.

This solubility can cause reliability problems due to embrittlement of the solder joint if the dissolved gold content is too high. An AuSn6 intermetallic compound forms which weakens the mechanical characteristics of the joint. This condition is seen as a dull, matte appearance of the solder, and is the primary reason behind maintaining the gold at the absolute minimum necessary to protect the nickel while operating at a manufacturable set of process conditions. For electrodeposited gold this minimum depends on cell geometry and line transport characteristics, as the minimum current density level necessary to activate the anodes tends to focus primary control of deposit thickness on immersion time in the cell. A common minimum is approx. 0.3 , and the applicable thickness spec is "gold flash: 0.5 ". It is recommended that a silver bearing paste (62Sn/36Pb/2Ag) be used when soldering to gold due to the tendency of the silver component to reduce the AuSn6 intermetallic formation, and that the gold be held to the minimum recommended above. Solder volume should be kept as large as possible, using a 0.2mm stencil thickness with no more than 75 difference between deposit width and pad width.

All commonly used flux types are compatible with soldering to nickel/gold finishes: the choice here depends on the user's cleaning requirements.

- Thickness Uniformity

For electroplated finishes the best results regarding thickness uniformity are obtained when the finish is "full" as opposed to "selective": only in the full gold process is a completely uniform buss structure available in the form of the copper foil underlying the electroplated circuit pattern. In the selective approach, the nickel and gold deposition depends on the existence of tie lines within the circuit pattern which will guarantee that the entire pattern is short circuited together. These invariably present different series resistances, with the result that it is difficult to obtain thickness distributions (primarily in the nickel layer) better than 60%, and excursions of three times the specified thickness are difficult to avoid in isolated areas. The presence of a uniform buss structure in the full sequence improves the tolerances to 30% or better provided that good design practice (minimum of isolated or "point" radiators, liberal use of thieving and hatched shield areas to balance current distribution) is followed. Further advantages to this approach are that the added complexity of tielines in the circuit is eliminated as is the need to drill or route out the shorting nodes during final fabrication. The disadvantage is that the use of a non-fusible overplate as an etch resist will leave an overhang on the conductor edge of up to the thickness of the base copper in width. This may cause encapsulation difficulties with dry film soldermask and may also provide point radiation problems at high (RF)

frequencies. A further concern at high RF is that the development of a "skin effect" in the conductor as the signal charge transfer moves to the outer perimeter of the line will cause changes in signal propagation characteristics due to the variation in resistivity between the overplate and bulk copper. At 900 MHz, the active area of the conductor is only about 5 microns thick, implying that the signal travels entirely in the overplate.

Immersion or electroless gold represents an alternative to electroplated gold in those cases where an alloy is not required for hardness or wear resistance. The electroless process deposits a thin (<0.1) immersion gold coating over a nominal 5 deposit of nickel-phosphorous alloy. The process requires activation of the copper surface: the palladium based catalyst enables selective deposition of the nickel and subsequently gold on all exposed copper surfaces. The electroless nature of this process guarantees both a very thin coating of gold and an effective planarity similar to that of the underlying copper deposit without the bussing problems of electroplated finishes.

4. Conclusion

Gold offers many advantages as a protective overplate in an assembly environment where eventual contamination of a wave solder line is not a problem. It is flat, inert, and non-fusible, and has excellent soldering characteristics under a variety of assembly conditions. AuSn6 intermetallic formation can be controlled through minimization of the gold content in the solder (minimize gold thickness/maximize solder paste volume), however critical applications should be characterized by vibration testing. The major disadvantage to its use in reflow assembly is cost, and a long term view should monitor other developments such as palladium nickel or copper/nickel/tin. A further disadvantage regarding FPT is the need for a deposit of solder paste: while this is an option at pad pitch of 0.5mm, it becomes problematic as pitches decrease to 0.4 - 0.3mm.

Reflowed solder finishes offer good potential for FPT assembly, however the total solder volume requirement needs to be well understood to permit both process and eventual facility definition. Initial work supported by IBM Canada[4] has applied the Laplace equation of capillarity to lead geometries typical of various FP packages (TAB, SQFP, etc). Considering the total solder joint volume required (as opposed to paste volume) for fillet heights from 0.2 to 0.3mm, respective volume requirements will be from 0.61 to 0.80mm^3. This represents a deposited solder thickness of 65 - 85 on a 0.25 x 1.5mm pad, assuming wetting requirements of the pad surface outside the immediate foot area of the device lead are negligible. Even so, these thicknesses are from 6 to 10X the values normally encountered in conventional subtractive processing. From a process standpoint, it will also be necessary to characterize finished reflowed solder thickness for various pad geometries, as the topography of the solder is strongly dependent on the relationship between the solder wetting angle and the pad dimensions in X and Y. While a nonreflowed finish does not present these problems, it is porous, subject to contamination during processing, and degradation of solderability as the lead component oxidizes.

Hot Air Leveling has not reached the end of its possibilities as a finishing technique, but vertical processes tend to be characterized by excessive variation at the current state of the art to be considered as a viable option for FPT. Horizontal offers significant potential.

Therefore a possible order of priority for FPT finish evaluations would be the following, in which process compatibility has been weighted slightly ahead of cost and flatness. Cpk is

used due to variations in applicable specs: the objective here was more to see how consistent each process was, and so the capability index is referenced against a tolerance field of 12 m. Fusible and nonfusible overplates are considered seperately due to the non-applicability of the capability index and fundamentally different approach to assembly processing represented, however the rating scheme used is the same.

4.1 Fusible Overplate Options for FPT

Process	Cpk	Process*	Cost	Rating**
Horizontal HAL	2.35	10	1.02	92
Photo Solder***	2.67	10	1.18	91
Reflowed SnPb	1.79	9	1.06	64
Nonreflowed SnPb	4.40	3	1.06	50
Vertical HAL	0.85	10	1.03	33
SnPb Paste (Panel)	0.48	8	1.06	14
4.2 Non-Fusible Finish Options				
Immersion Gold	—	10	1.16	208
Electroplated Gold	—	8	1.25	153
Passivated Copper	—	6	1.00	144

* Process compatibility index: 10= no impact/minimal changes required to introduce

** Weighted index. Maximum (Cpk=6.00, Process= 10, Cost = 1.00): 240

*** Estimated values

Based on the analysis presented earlier in this report and the relative weights given to flatness (30%), process compatibility (40%) and the relative cost of pwbs manufactured using the various processes (30%), the clear choices are horizontal hot air leveling or the photosolder process if the assembler requires a fusible overplate. In the case of the photosolder process, this affords the possibility of eliminating solder paste printing during assembly. The most cost/performance effective finish amoung those looked at so far for pwbs going into an FPT assembly process using solder paste is immersion gold.

Acknowledgement

The author wishes to thank Mike Weinhold of DuPont for valuable insights into the new technology of "Preformed Solder Deposits" which aided in preparation of this paper.

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HOW COMBINATION OF MCM AND LTC MEETS THE INDUSTRIAL MOBILE COMMUNICATION REQUIREMENTS

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Some years ago new materials appeared which modified fundamentally the concepts and industrial processes in the hybrid integration world. The "Green Tape™" is what we are going to deal with in this paper.

For four years SOREP and DU PONT DE NEMOURS have established a close partnership to develop and industrialize this new product. As a result it will be possible to manufacture as soon as the beginning of 1992 a large volume of these low temperature cofired (LTC) ceramic substrates with increased performances at a moderate cost.

When it is finished, a LTC substrate looks like a common alumina substrate on which all common operations of thick film technology may be performed (i.e. screen-printing of resistive pastes or conductive pastes as well as die attach, bonding or SMD brazing). In fact, this substrate is made of the stacking up of several tapes on which vias are formed and conductors are screen-printed.

At this stage, let us make a rapid comparison which shows that the LTC substrate is at an intermediate level between the PC board and the common thick film alumina substrate.

Figure 1 shows transversal sections of the three above mentioned substrates. The PC board is characterized by independent and stacked sheets of insulating material (epoxy glass), each of them supporting an etched conductor layer. The common thick film substrate is made of an alumina plate on which are alternatively screen-printed insulating and conductive layers. Insulating layers contain some holes (or vias) which are filled with conductive paste to connect two adjacent conductive layers. The LTC substrate is a stacking up of independent and insulating sheets (green tape) supporting screen-printed conductors, that makes it conceptually similar to the PC board. However conductive layers are connected with vias filled with conductive paste and therefore it has technological similarities with the thick film substrate.

Basic materials used for LTC manufacturing are obviously the tape and the conductive pastes.

The tape is initially conditioned in 44 inches x 300 foot rolls and may be cut and delivered in rolls adapted to the substrate manufacturing tool. Several thicknesses are currently available: typically 4½" (115 μ), 6½" (165 μ), 12½" (315 μ). The tape is composed of a mineral phase (alumina grains with glass phase), an organic phase (acrylic resin based) and solvents.

The conductive pastes are of two types: standard pastes which are used after cofiring for external screen-printing (Au, Ag/Pd, Au/Pt/Pd) and special pastes used before cofiring for internal conductors and vias screen-printing (Ag, Au, Ag/Pd).

The substrate manufacturing flow-chart set forth in Figure 2 shows the main steps of the industrial process and points out its advantages if compared with the manufacturing process for common thick film substrate.

The first step consists of separating the basic sheets, which are obtained by cutting the tape to proper dimensions using a compound die. Registration and orientation marks may be punched simultaneously. Each sheet is then drilled or punched to form the vias and receives two screen-printing operations (via filling and conductor printing) and a quality control.

Two significant advantages of the process can be mentioned at this stage:

- first, thanks to the flexibility of the basic material, punching can be used instead of drilling like for PC boards, thus saving much time and cutting costs down;

- second, because sheets are independent, screen-printing operations may be conducted in parallel without intermediate firing whereas these operations are necessarily serialized for common thick film substrates.

These two features allow to reduce drastically the manufacturing cycle of the LTC substrate which duration can be as short as for the PC board. As far as common thick film is concerned, we can also note that the independency of printed sheets involves a significant cost reduction since a defectuosity on one sheet does not lead to a rejection of the complete substrate.

The third step corresponds to the assembly operation (collating and lamination) leading to the manufacturing of a monolithic but flexible substrate due to its organic constituents. After cutting or scribing, burn-in and firing operations are performed with a view to remove any solvents and organic constituents so as to obtain a rigid substrate.

Among the most significant advantages of the process, it is worth mentioning the complete automation as well as a strong modularity. Taking these points into account, SOREP decided to set up an automated production line with cassette transfer between the machines. To tell the truth, prices are even competitive when comparing with PC boards for some applications. By the way, costs can also be lowered by the use of silver conductive layers, whatever their number.

Another attractive characteristic of LTC substrates is the possibility of obtaining at a reasonable price a double-sided substrate with a hermetic separation between the two sides while maintaining lay-out density. Indeed, contrarily to metallized holes in PC boards or standard alumina substrates, vias do no take additional place compared to the tracks.

The attached table set forth in Figure 3 sums up and compares the electrical and mechanical characteristics of the LTC substrate with other ordinary technologies.

- Electrical characteristics

Let us consider the capacitive aspects. With a dielectric constant of 7 and a distance between layers ranging from 100 to 250 μm, the LTC grants coupling capacities lower than 0,05 pf per crossing. The use of silver for connections from one layer to another through filled vias and for conductor tracks involves a low resistivity (about 100 mΩ/cm for 250 μm tracks). This shows clearly that frequency operating limits are very high, which we can demonstrate with the 2 following examples:

1- SOREP has developed large hybrid memory maps on LTC substrates on which conductors lower than 1 pF have been added. The address and data buses allow to benefit from the highest performances of basic dice.

2- SOREP is currently carrying out investigations on 622 Mbits hybrids dedicated to telecom applications. In this case, the only necessity is to care for routing, not to adapt most of ECL signals.

As to the physical and mechanical aspects, one can add the possibility of manufacturing substrates with an almost unlimited number of layers while keeping costs down (see figure 4). In fact, the cost of a cofired substrate does not rise exponentially with the number of layers for the difficulties due to the positioning of layers are not cumulative and the yield of final assembly and firing operations is very high.

Moreover, as it is easy to cut green tape foils and thanks to the hermeticity of the material after firing, we can envisage interesting developments at the integration level. We can give some examples:

- The realization of specific PGA by pin brazing at the back of the substrate.
- The manufacturing of 3D circuits with the integration of cavities, walls or columns.
- The complete packaging integrated into the module by use of an adhesive or brazing of a ceramic or metallic lid onto the substrate similariy to high temperature cofiring technology.
- Heat dissipation in the best possible conditions by use of an adhesive or brazing of a heat sink on part or whole substrate.

What about the current needs in modern radio telephone techniques today? This market will be dominated by portable, low cost and widely spread equipments. To these industrial features, following functional characteristics can be added: these equipments will progressively include all telecom areas, from speech to image transmission through data and telefax. Some articles in the press already quote investigations on the "pen telephone" or "pocket fax". This is the evidence that miniaturization will play a determining role on this particular market.

At SOREP, we believe such a miniaturization at a cost compatible with the industrial features of this market can be reached with two important technological concepts: the MCM (multi-chip module) and the LTC.

The common point of these new equipments is the intensive use of digital signal processing circuits. Now, it will take a long time before a sole monochip can perform all tasks, from protocol management to user interface management via signal digital filtering, data compression, information storage, operation reliability, auto-diagnosis etc.

It seems thus obvious that for some more years circuitry will need a considerable more or less specific (ASICs) number of dice (10 to 30).

In the same way, there will be a great number of tricky interconnections: the widening of data buses to 16, 32 and even 64 Kbits and the acceleration of the operating frequency are generally the first solutions to be implemented to increase signal processing performances while saving the surface of active silicon.

The MCM meets the above mentioned needs by gathering together all individual dice under the form of a unique component with high density integration, which improves the reliability of the whole function, reduces the assembly costs and takes the miniaturization constraints into consideration. It still assumes that the substrate allowing the interconnection between dice offers the same advantages. We believe this is the case of LTC.

The bonding of dice on alumina is a process, the reliability of which has already been demonstrated. Indeed, it has been used in most of the products devoted to run in severe environments. As already stated above, the interconnection complexity does not involve an exponential increase of the LTC substrate cost. That is why this is particularly interesting in the case of complex MCM like those to be used in phone pocket terminals.

Regarding the intrinsic electrical features of the cofired substrate (low coupling capacities, low track resistance and low serial inductances due to short connections) and the possibility of integrating ground and power planes at low cost, we expect digital circuits to run at a very high frequency, with a minimum of decoupling capacities and signal adaptation, thus enabling size and cost reduction while increasing performances.

Furthermore, with regard to drilling and substrate cutting facilities before firing associated with brazing or reflow operations, it seems that the modules developed with this technology will both support various connection technologies (flex, leads, pins, connectors etc). In the future, in accordance with the new ergonomy constraints and also to follow the fashion in this area, they may be integrated in complex shapes of substrates similarly to PC boards.

As a conclusion, if MCM are necessary to meet the miniaturization and complexity needs of portable telecommunication products (pocket telephones, portable faxes, mobile terminals, etc.), no doubt that their introduction on the market will demand performant and cost effective technologies.

Following several investigations we do believe that the LTC technology has the necessary qualities to fulfill these requirements:

- a reasonable cost of basic materials;
- the possible advanced automation for mass production;
- a final cost rising slower than complexity;
- capacity of integrating both packaging and connection;
- high electrical performances;
- possibilities of on line test and repairing after cabling;
- high reliability.

We think that the work which is now being performed and which will be carried out in the near future at SOREP will bring further evidence of the interest of such a technology.

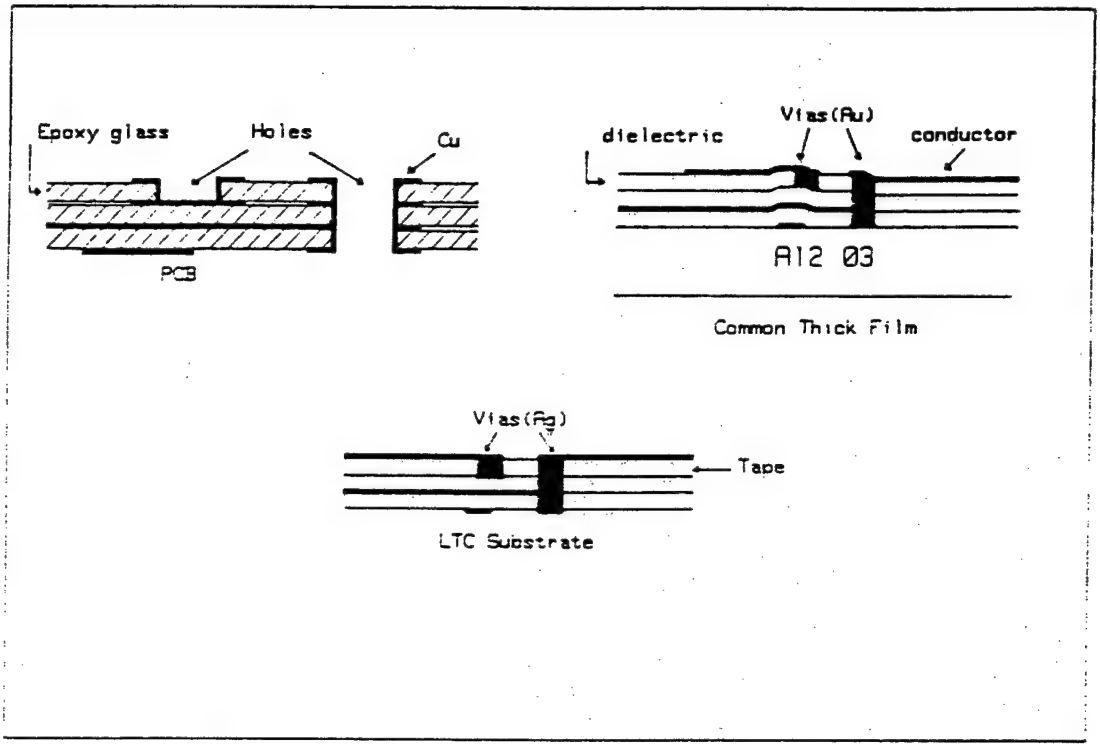

Figure 1

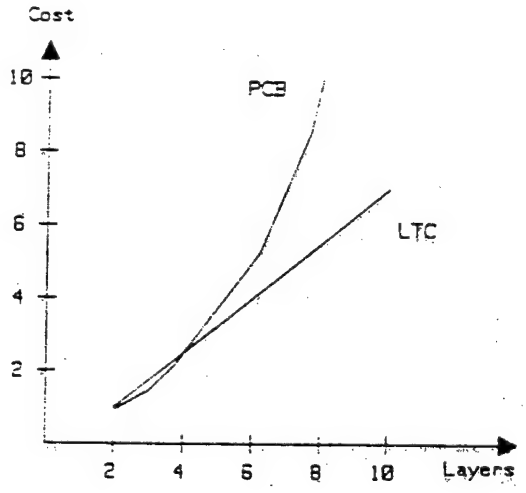

Figure 4

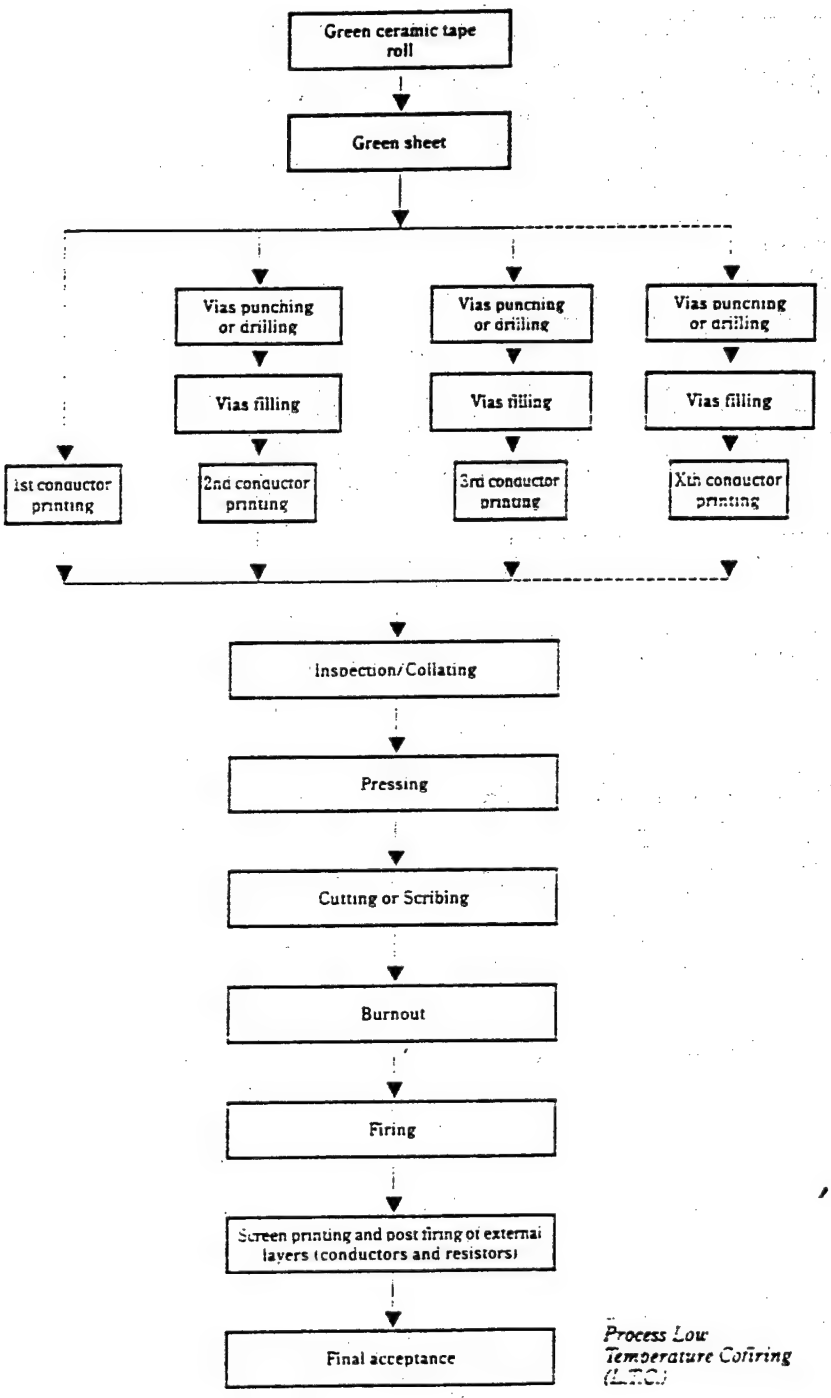

Figure 2

LTC manufacturing flow-chart

Features	M.T.F.	H.T.C.	L.T.C.	Advantages LTC/MTF	Advantages LTC/HTC
Cofiring temperature	< 1000 °C in air	> 1500 °C in reducing atmosphere	< 1000 °C in air		MTF standard furnace: Cost reduction
Manufacturing process	Serial	Parallel	Parallel		
Number of screen printings per conductive level	4	2	2	Cost and Delivery Time Reduction	
Number of firings (before external screen printing)	Several	1	1		
Internal conductive layers	Au (< 5 mΩ/□)	W or Mo Mn (15 mΩ/□)	Ag (Au for special applications) (<5 mΩ/□)	Costs reduction	Lower resistivity Voltage drop and propagation time reduction
Dielectric constant	-	9-10	-		Crosstalks and propagation time reduction
Dielectric thickness	40 µm	Variable	90 µm or more	Crosstalks reduction Increase of dielectric strength	
Shrinkage	No	High	Low	Increase of density	Better accuracy
Connection between sides	Metallized holes	Vias	Vias	Increase of density	
Number of layers	6 max (standard)	Unlimited	Unlimited	Increase of density Flexibility	
Screen printed resistors	Yes	No	Yes		Cost reduction Flexibility Increase of density
3 Dimensions (3 D)	No	Yes	Yes	Flexibility Increased packaging capabilities	

Figure 3

Features and advantages of LTC technology

FINE-PITCH PLACEMENT IN THE SMT PROCESS

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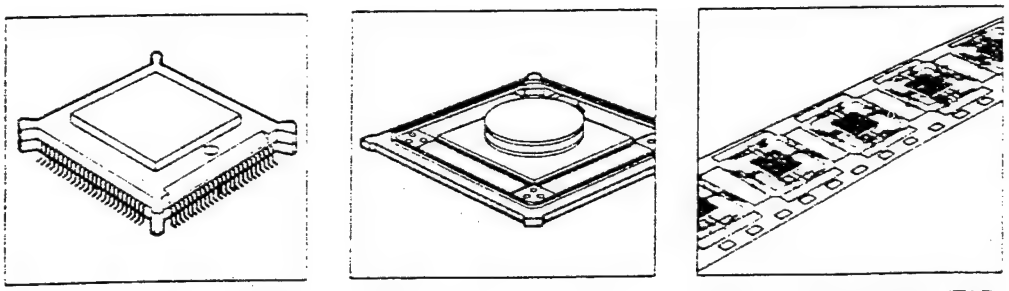
1. Introduction

Market pressure on the electronics industry to improve products in terms of processing speed, size, quality and price remains undiminished. The consequent increase in the level of integration seen in integrated circuits is giving rise to a reduction in lead pitch sometimes combined with a dramatic increase in lead count. Technological difficulty in the Surface Mount Technology (SMT) area is automatically increased as a result. This paper is intended to provide an overview of the essential elements of the SMT process sequence.

In general, the term fine-pitch components is used to describe components with a lead pitch of 25 mil (0.635mm) or less. For lead pitches significantly below this level, the terms ultra or super fine-pitch are used. The technology required for the processing of fine-pitch components is frequently known as fine-pitch technology (FPT). FPT is the central area for innovation for Surface Mount Technology.

2. Typical Fine-Pitch Package Forms

The most common fine-pitch component package forms currently in use are the Flat-Pack (FP) and the Quad Flat-Pack (QFP).



Plastic Quad Flat-Pack (PQFP) with heat sink

Molded Carrier Ring (MCR)-family such as TapePak

Tape Automated Bonding (TAB) such as Mikropack

Figure 1: Fine-pitch package forms

With TABs (Tape Automated Bonding), a die is connected with an etched connector pattern on a carrier film using an inner lead bonder (ILB) which generally operates using the hot-bar soldering principle. TABs have been in use in high volume for years in Japan and in smaller volumes in the USA. Until now, TABs have had a comparably low significance in Europe. In the USA and in Europe, a recent trend is apparent towards MCRs corresponding to the JEDEC

norms. The ends of the IC connector leads are, in this case, molded in a plastic casing frame (Molded Carrier Ring). MCRs are currently available in stick or stack magazines and in 8 different standard frame sizes (16mm x 16mm to 86mm x 86mm). A range of further package variations, especially for memory ICs, are expected on the market, e.g.:

TSOP - Thin Small Outline Package
TQFP - Thin Quad Flat Package
SQFP - Shrink Quad Flat Package

3. Key Performance Factors and SMT Process Steps

Against a background of increasing product liability and increasing pressure on the suppliers of electronics products to reduce costs, the right quality philosophy is essential. In the high-tech sector where fine-pitch technology is being applied most intensively, one objective must be to achieve the highest possible level of statistically based 'manufactured' quality (see Section 4 - Machine Capability). The correction of localized manufacturing faults within a high-cost functional test repair loop can be very critical, particularly for highly sensitive, sometimes expensive fine-pitch components. The quality, in general, of products manufactured using the SMT process and the FPT process is determined primarily by a number of factors within the different process stages:

* PCB and component tolerances (see Section 3.1)
* Solder paste application (see Section 3.2)
* SMD placement (see Section 3.3)
* Reflow soldering (see Section 3.4)

Maintaining the desired quality standards requires a range of quality feed-back loops which should be as short as possible. If such feed-back loops are not already in operation in the corresponding placement systems, subsequent integration can be immensely beneficial.

3.1 PCB and Component Tolerances

The dimensional stability of PCBs and components naturally has a strong influence on product quality. This can be illustrated with an example of tolerance analysis for the placement of a fine-pitch component with 20mil (0.508mm) lead pitches :

Lead pitch (component):	TLP approx. +/- 0.035mm
Lead width (component):	TLW approx. +/- 0.010mm
Pad pitch (PCB):	TPP approx. +/- 0.010mm
Pad width (PCB):	TPW approx. +/- 0.010mm
Local fiducials (PCB):	TLF approx. +/- 0.010mm

The quadratic combination of these tolerances is as follows:

$$T(TOT) = \sqrt{TLP^2 + TLW^2 + TPP^2 + TPW^2 + TLF^2} \approx 0.04mm$$

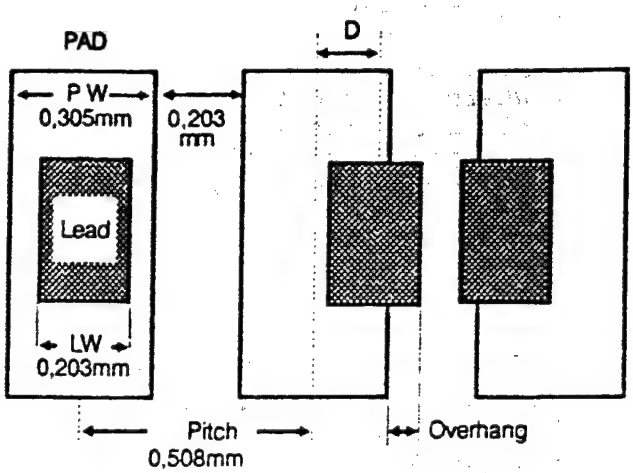


Figure 2: Lead - pad deviation

In the majority of situations, guidelines are applied such that the lead overhang should at most correspond to 1/3 of the width of the lead itself. The max. permissible deviation in this case is therefore:

$$D = PW/2 - LW/2 + \text{Overhang} = (0.305/2 - 0.203/2 + 0.203/3)\text{mm} \approx 0.12\text{mm}$$

The remaining deviation from the placement system is therefore:

$$DP = D - T(TOT) = 0.12\text{mm} - 0.04\text{mm} = 0.08\text{mm}$$

3.2 Solder Paste Application

In spite of isolated, determined attempts to apply the wave-soldering process to fine-pitch technology, the conventional process looks as follows:

- Solder paste application - SMD placement - Reflow soldering

For the application of solder paste in SMT mass-production, there are two methods which merit discussion: screen or stencil printing

The central element of the screen printer is the screen which generally comprises a stainless steel or polyester mesh covered with a polymer coating. The main screen parameters are the mesh density and the screen thickness. A characteristic of the screen printing method is the use of a process-dependent distance between the application surface and the screen (snap-off).

For fine-pitch technology, the stencil printing is clearly preferable because of the higher edge definition of the stencil. Print patterns in stencils made of stainless steel, nickel silver, bronze, copper beryllium or similar materials are almost generally produced by an etching process. The highest printing precision is achieved through the use of screens cut by laser. The screen openings should be approx. 10 - 15% smaller than the corresponding pads on the PCB. During the printing process, the screen generally lies in contact with the PCB (on-contact).

In comparison with screens, stencils have the following advantages:

- Long life
- Where component variety is high, stepped etching can allow different application thicknesses. In that case the hardness and pressure of the squeegee have to be adjusted precisely corresponding to the position and height of the etched edges

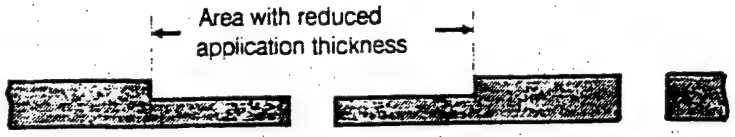


Figure 3:
Stencil with
stepped etching

One of the most important objectives for solder paste application must be to avoid the formation of bridges during the subsequent soldering process. One possibility for reducing the risk of bridging in fine-pitch applications is to employ a zigzag-print pattern on the pads. This technique does, however, require longer foot length.

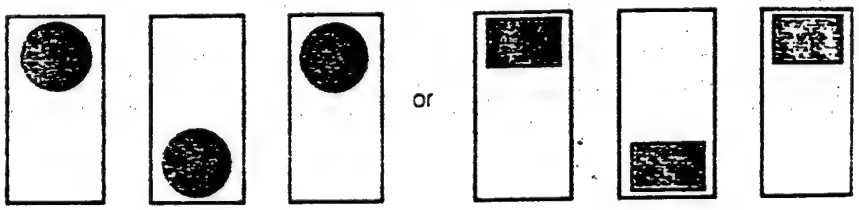


Figure 4:
Alternative
print patterns

A major influence in the quality of the solder paste application results is the precise alignment between the PCB and the screen. The best reproducability with limited accuracy (typically 0.05mm on a 3-sigma basis) is, without a doubt, achieved by solder paste application systems with vision capability.

A significant factor in the determination of the final solder quality at the end of the conventional process chain is the selection of suitable solder paste.

The Inspection of Applied Solder Paste

The producer of high quality, high value electronic products must consider the use of quality assurance systems such as automatic solder paste inspection systems.
Depending on the requirements such systems are based on the measurement of shadows, produced by a variable flashing or the triangulation principle (for precise height measurement of the solder paste deposits).
In certain instances, the suppliers of solder paste application systems are already offering the option of integrated solder paste inspection systems. The level of inspection accuracy available in such cases will almost certainly be unable to match that of the specialist systems.

3.3 SMD Placement Systems

As a result of the diverging trends in the component sector (small components are becoming ever smaller, fine-pitch components are becoming ever finer), enormous demands are now being placed on the second element of the conventional SMT process sequence, the SMD placement systems. Very generally, four main categories of SMD placement machines have developed over the last few years:

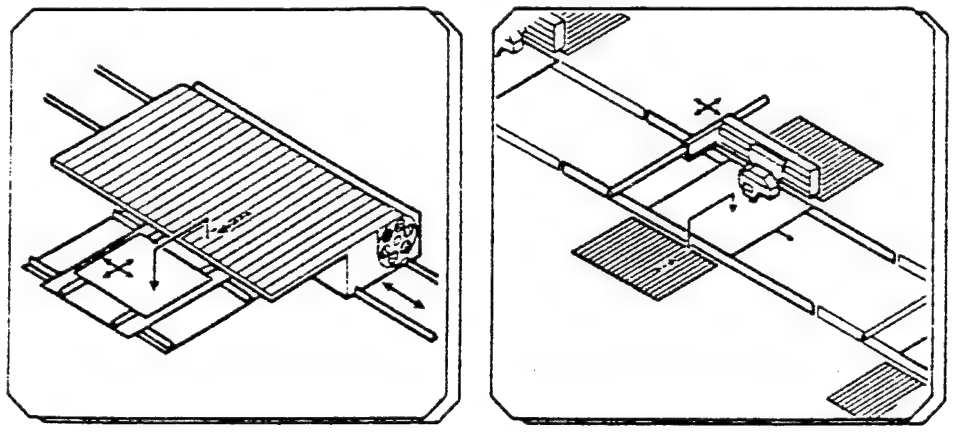
- Entry level systems based on the pick and place principle, with limited performance and accuracy.

- High-performance placement systems equipped with revolver heads for the processing of small chip components as well as fine- pitch ICs with 25mil lead pitches and a max. size of 32mm x 32mm.

- Simultaneous placement systems for the mass processing of small chip components and ICs with coarse lead pitches.

- Fine-pitch placement systems for IC components with lead pitches of 15mil (0.381mm) and, in individual cases down to 12mil (0.305mm), and with edge dimensions up to 50mm. These machines are sometimes capable of placing the smallest chip components with edge dimensions down to 1mm x 0.5mm (0402).

Fine-pitch placement systems can only operate optimally using the pick and place principle (2 main variants). This necessity arises out of the need to handle each component individually in terms of positioning dynamics, force sensors and special sequences during the opto-electronic vision and coplanarity measurements.



Moving PCB and feeders Stationary PCB and feeders

Figure 5: Pick and place concept variations

From the two competing concept variations, the system with both stationary PCB and component feeders offers significant advantages compared with the alternative. The stationary PCB ensures that previously placed components are not displaced. Stationary component feeders ensure that component replenishment is possible during machine operation which contributes to high utilization levels.

In terms of the performance data for fine-pitch placement systems, the most significant aspects without a doubt relate to placement accuracy and placement reliability. The principal factors in this respect are:

- Drive and path measurement principle, resolution in the relevant NC axes including X, Y and theta.
- Distance between the X-Y guide plane and the PCB plane
- Mechanical construction of the placement head.
- Vision systems for the opto-electronic centering of components and PCB

Consistently high positioning accuracy in the X-Y axes can only be achieved with the use of direct path measurement using linear path measurement systems (e.g. glass scales) (see Figure 6). The positioning control system can determine the position of the placement head throughout the complete positioning sequence and can hence react accordingly.

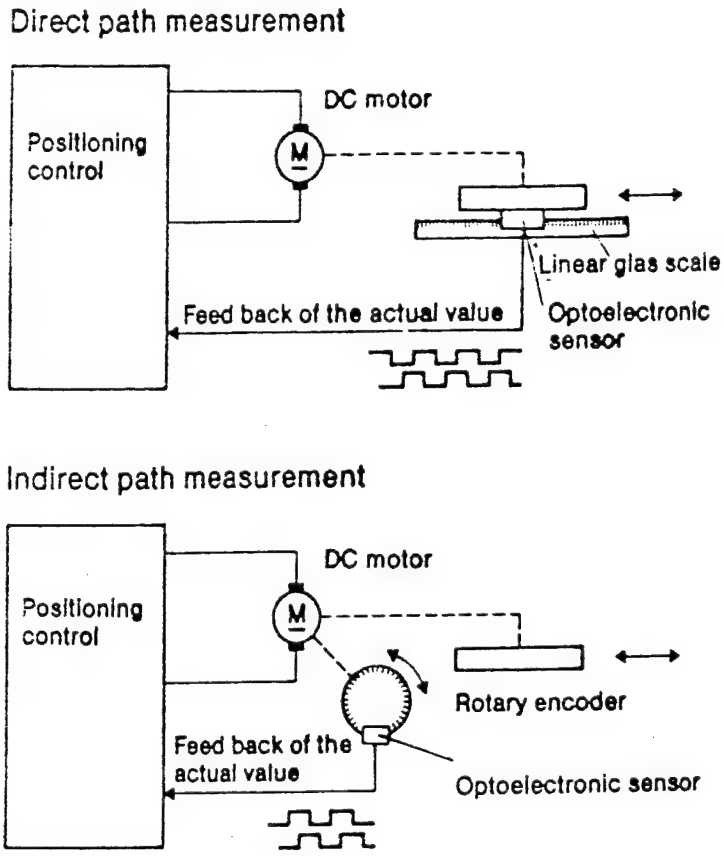


Figure 6:
Path measurement principle in SMD placement systems

The use of rotating measurement systems coupled to the X-Y drive motors can be described in an extreme manner as: MEASUREMENT AT THE WRONG POINT. All errors relating to mechanical play and wear in the drive system have an adverse impact on placement accuracy.

Direct path measurement is also preferable to indirect methods for the high accuracy rotation axes for vacuum nozzles. For the precise placement of fine-pitch components, a resolution for the X-Y axes is required of at least 10µm.

A basic requirement for the achievement of high placement accuracy in automatic placement systems is the precise centering of both PCB and components. Mechanical centering devices are no longer sufficiently reliable for applications involving fine-pitch technology. The integration of a high performance vision system is therefore essential.
Some important distinguishing parameters for vision systems are:

- Binary or grey scale system
- Lighting method
- Image processing method
- Measuring accuracy

A major factor in determining the reliability of vision systems is the vision processing method used. The two main competing types are the centre-of-gravity and correlation methods.
Due to a low sensitivity to changes in brigthness the grey scale system has clearly succeeded over the binary system. Regarding the component vision centering the incident lighting is to be prefered in comparison with the through ligthing. The real contact area of J-leaded ICs can only be measured by applying incident light from below.
As a result of the high reliability, the correlation method is to be recommended. The point of maximum correlation or congruence in terms of the actual and nominal images determines the required position. Factors which can partially alter the appearance of the object have no negative impact on the accuracy of component placement. As a result, this process also allows the use of non-homogeneous and asymmetric fiducial markings. The measuring accuracy for vision systems for both PCB and component centering should be approx. 20µm.

Figure 7:
Correlation principle

In current discussions concerning component vision, the term 'lead-to-pad matching' sometimes crops up. With this form of component centering, the IC is brought to a position where the lead structure is matched directly against the corresponding pad structure. The component is then lowered onto the PCB. Lead-to-pad matching would certainly provide a method of placing fine-pitch and super-fine pitch components accurately even when the basic mechanical machine accuracy is limited. Unfortunately, there are two major hurdles which are currently preventing the application of this process to SMD placement systems:

a. The integration of a camera and lens system into the placement head which provides a parallax-free image of the leads of different sized components.

b. The applied solder paste layer can alter the image of the pad structure.

At this point, it is also appropriate to mention a further important aspect of fine-pitch placement technology - component lead coplanarity inspection (see Figure 8). Using a coplanarity module integrated into the SMD placement machine, lead planarity errors can be detected with a high degree of resolution. Scanning of the individual leads is carried out sequentially with the component being traversed through a fixed laser beam whilst held on the vacuum nozzle. Measurement is based on the triangulation principle with the reflected laser light being used to generate a height-dependent signal in a PSD element (Position Sensitive Device) or a CCD chip. Using special processing algorithms, the correct placement plane is determined (based on 3 leads). The placement plane represents the reference plane for the programmable tolerance band for vertical lead skew. The level of acceptable vertical lead skew is proportional to the thickness of the applied solder paste layer. The adoption of PCB tolerance rejection criteria is recommended in the case of large ICs and where quality requirements are high.
It should be taken into consideration that PCB warpage will reduce the width of the tolerance band for the vertical lead skew. Coplanarity measurement using a laser has the advantage over the other shadow-based camera methods of considerably higher accuracy. Accuracy levels in the region of 10µm are already attainable.

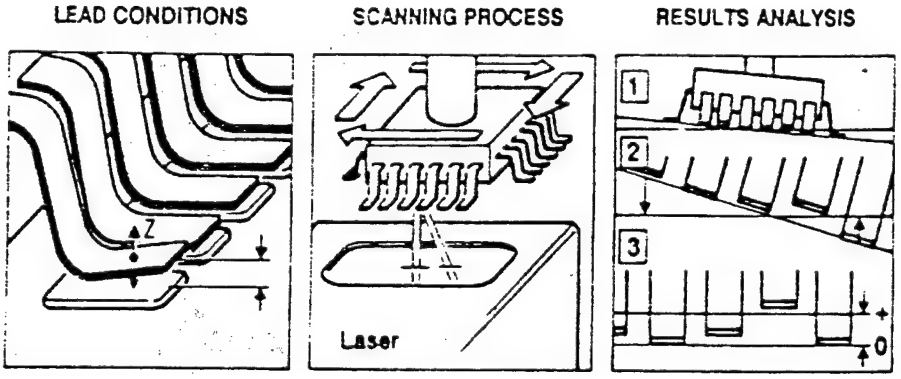


Figure 8: Coplanarity lead inspection

A particularly difficult problem for the supplier of fine-pitch placement systems relates to the processing of TAB and MCR components. The extraction of ICs from the carrier along with the subsequent forming of the connector leads into the required format are being increasingly tranfered from the IC manufacturing process to the SMD placement process. This is a beneficial development as a range of handling steps are eliminated which would otherwise have an adverse impact on quality. The price for this improved quality, however, must be paid by the fine-pitch user in terms of higher component feeder costs. For MCR components, there are basically three different feeder concepts:

- Integrated feeding out of one magazine of one supply format
- Integrated feeding out of several magazines of one supply format
- Separation of the feeding and excising/lead forming functions with the objective of maximizing overall cost effectiveness by increasing the utilization of the expensive excising and forming tools.

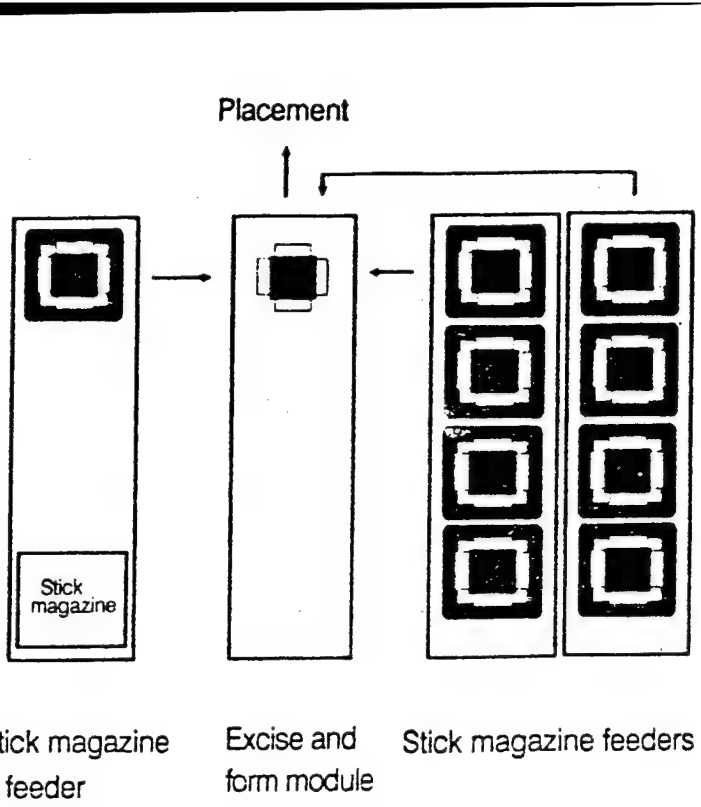


Figure 9:
MCR processing in fine-pitch placement

3.4 Reflow Soldering

In order to successfully complete the final stage in the SMT process, reflow soldering, the user has the difficult selection to make of a suitable reflow soldering unit. For mass reflow soldering, there are more or less four different processes:

- Vapour phase (VP)
- Infrared (IR)
- Infrared with additional forced convection
- Inert gas

With vapour phase soldering, the object to be soldered is brought into a zone of saturated vapour from a boiling primary medium at 215 °C. The solder energy is derived from the almost immediate condensation of the primary medium. The heating of all solder joints to exactly 215 °C, even in the case of widely differing component sizes, is a major advantage of this process.

Vapour phase soldering does, however, have a few serious drawbacks:

- Thermal stress for components resulting from the rapid temperature change. This effect can be diminished using a preheating of the PCB to be solderd.

- The required chemicals are environmentally unfriendly and, under certain circumstances, can be highly toxic.

- Operational costs are high through the unavoidable loss of the expensive primary medium.

In the case of IR reflow soldering, energy transfer occurs principally via radiation and, to a smaller extent, via convection. IR soldering systems available on the market are equipped with radiation elements of different wave lengths. The biggest problem

with pure IR solder systems is the variation in radiation absorption properties in the different materials and in the surface of the solder deposits. As a result, reflective surfaces such as pads heat up much more slowly than the majority of black IC packages. For circuit assemblies with component types varying from the smallest SMDs to large fine-pitch components, temperature differences as high as 50 to 70 °C are possible. As the temperature profile must reach the required critical temperature even at the coldest point, temperature-related stress can reach critical levels for fine-pitch components in the hotter zones.

A much improved temperature distribution can be achieved amongst the solder joints using IR reflow soldering in conjunction with forced convection. With the introduction of suitable air streams or air agitation, the well-known problem with radiation systems of shadowing can be mostly overcome. With this method, block capacitors below large-bodied ICs can be satisfactorily reflow soldered. The use of air as a heat transfer medium has the disadvantage, however, that the unwanted surface oxidation of solder paste and pretinned pads and leads is actively promoted.

The best soldering results are achieved with convection reflow soldering ovens with an inert gas atmosphere (nitrogen). An important aspect of forced convection systems is that certain components, e.g. MELFs, can be displaced under adverse conditions as a result of the air streams present.

So far in this paper, a range of criteria have been discussed which are relevant to the placement accuracy of fine-pitch placement machines. The following section should clarify the basic concepts underlying future specifications concerning placement accuracy from the suppliers of automatic SMD placement systems.

4. Machine Capability for Automatic SMD Placement Systems

Amongst high-tech users currently, there is an increasing tendency to demand information from suppliers concerning the capability of machines or even of complete processes. A statistical machine capability analysis carried out by a supplier of automatic SMD placement systems provides a precise statement of the probability with which components will be placed within specified limits. The current status whereby data concerning placement accuracy is published in brochures and data sheets without reference to the distribution of results (multiples of the standard deviation) is unlikely to continue in the long term.

Standard Deviation

The arithmetic mean $\bar{x} = 1/n \sum_{i=1}^{n} x$ of the positioning cycles

together with the resulting mean deviation represents an unsatisfactory statement concerning placement accuracy. Figure 10 shows, for example, a possible distribution of the deviations in position of standardized components placed on a standardized substrate.

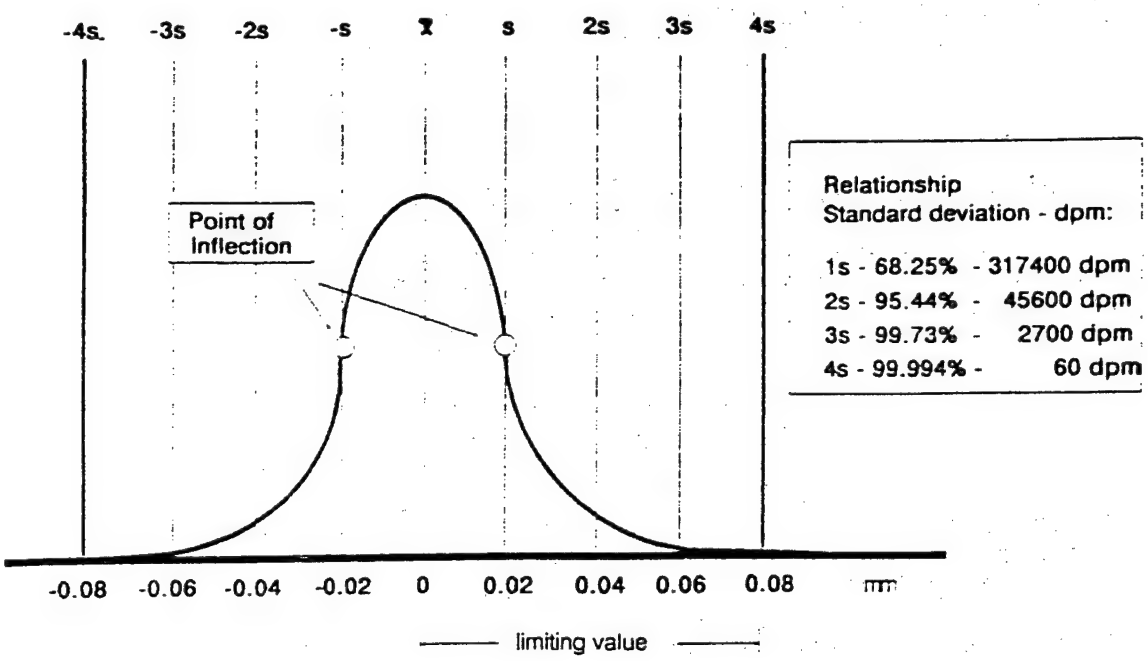


Figure 10: Normal distribution (Gaussian bell curve)

As positional deviations are generally distributed normally, the Gaussian bell curve provides an appropriate mathematical definition of the distribution. The distance between the two points of inflection and the centre line, the so-called standard deviation, is mathematically determined as follows:

$$s \text{ or } \sigma = \sqrt{\frac{1}{n-1} \sum_{i=1}^{n} (x - \bar{x})^2}$$

The standard deviation in the example in Figure 10 is 0.02mm. Expressed statistically, this means that 68.26% of all placements will have a deviation from the mean of 0.02mm or less. The distribution in the example can also be interpreted in the way that a component with a maximum positional tolerance of 0.08mm (see Section 3.1 - PCB/Component Tolerances) can be placed on a statistical base of 4 sigma. This is equivalent to a placement reliability of 60 dpm (defects per million).

5. Limits to Conventional SMT - Alternative Process Solutions

It is true to say currently that only very few users have reliably mastered the coventional high-volume SMD process for components with lead sitches of 20 mil (0.508mm). The main limiting factors are:

- Accurate and consistent solder-paste application in the 100µm region and below (also for uneven PCBs)
- Coplanarity of fine-pitch components in conjunction with PCB unevenness

5.1 Hot-Bar Soldering (Gang Bonding)

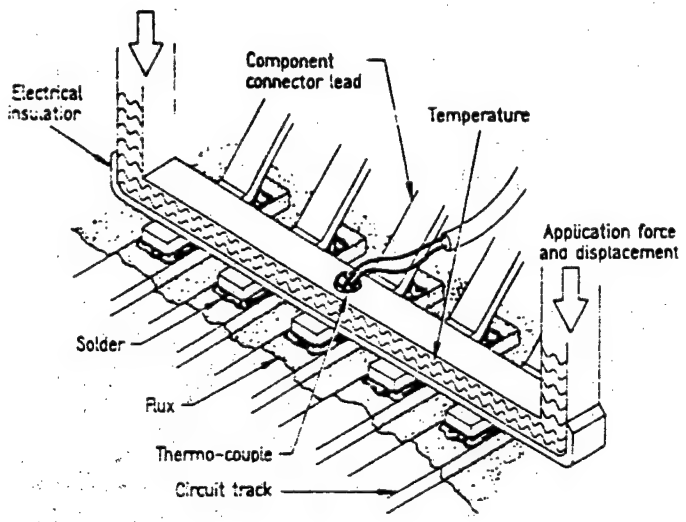


Figure 11:
Hot-bar
soldering principle

In the past, hot-bar soldering (or gang bonding) was carried out as a hand operation and, to a more limited extent, as a semi-automatic operation. The current trend is firmly towards fully-automatic, in-line compatible hot-bar soldering systems.

The basic design of a hot-bar soldering system is very similar to that of an automatic SMD placement system. The two main differences are:

- The standard SMD placement head is replaced by a special placement and soldering head in which the solder tooling is typically suspended by a gimbal and has a Z-axis positionable soldering tool.
- Freely programmable solder generator consisting of a PID controler and a heating power stage

The key steps in the process sequence:

After the PCB has been transported into the working area of the placement and solder head, automatic registration of the PCB is carried out by the vision system. Following retrieval from the feeder module, the component is first centered by the vision system relative to the solder-head and the corresponding pad structure and is then placed in position with the aid of a sensitive force sensor feedback system.

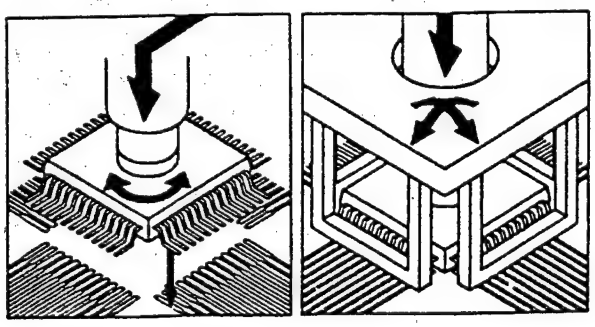


Figure 12:
Place component
and lower soldering tool

In the next step, the component-specific solder tool (can be changed automatically) is lowered onto all component connector leads simultaneously. After the required application force has been attained, the heating cycle is activated which follows a freely-programmable temperature profile. The solder head adapts to the soldering plane via a mounting based on a virtually frictionless gimbal. The centre of rotation of the mounting lies in the soldering plane thus preventing the transmission of lateral forces to the IC connector leads. The system can recognize the commencement of the reflow process from a small lowering of the solder head (in the range of µm) and can hence trigger a defined final soldering period (Figure 13). Soldering is always achieved with the minimum of heat energy which ensures that the growth of the intermetallic zone is minimized.

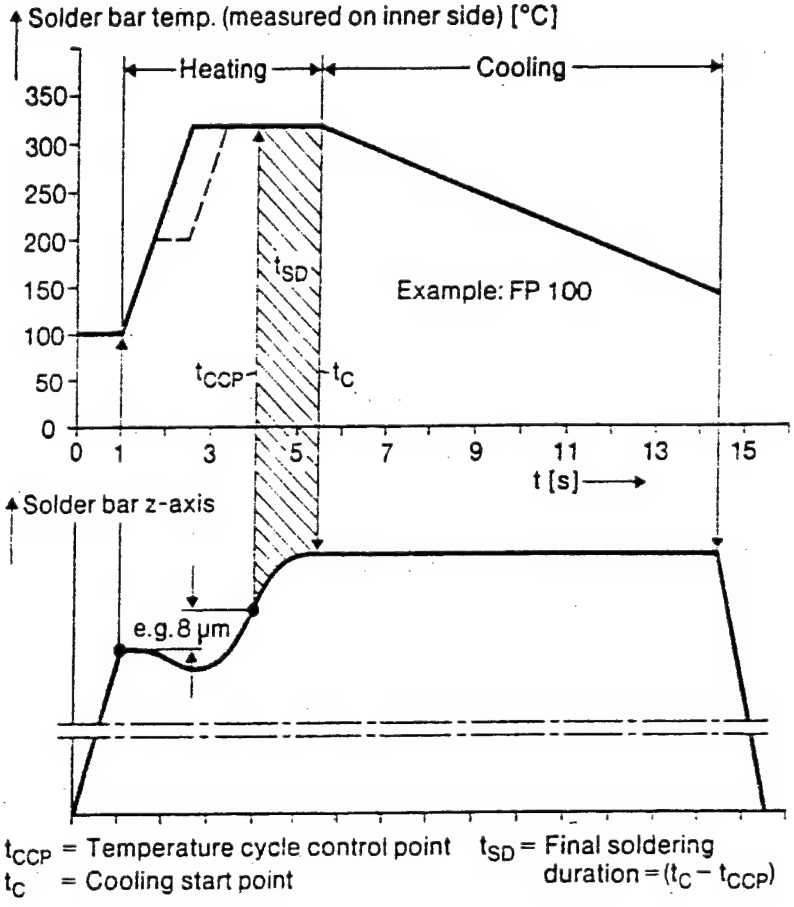


Figure 13: Relationship between temperature profile and solder head displacement

After expiry of the final soldering period, the solder-bar heating is switched off and the cooling of the solder head and the solder joint is then activated. Once the temperature of the joint falls below the solder solidification temperature, the solder head can be raised and the placement and soldering cycle hence completed. The total placement and soldering cycle time is dependent upon the component and PCB but is typically of the order of 20 to 30 secs.

During the soldering process, the component remains fixed in position and all flux fumes are extracted.

The use of an activator (e.g. flux) is practically in any case reqired. The selection of the appropriate application method depends to a high degree on the product reqirements. The flux for example can be applied to the component lead structure or to the pads on the PCB.

Major advantages of the hot-bar soldering process:

* Automatic planarization of the component leads

* Minimal thermal stress for components

* Individual treatment of each component type in terms of the programmable solder head parameters temperature, force and soldering tool displacement

* Reversal of the solder process also allows desoldering

Optimum processing of fine-pitch components in the hot-bar soldering process requires the adoption of special PCB layout guidelines. The ideal IC lead form is normally considered to be the so-called 'gull-wing'. Extremely flat TABs can also be processed without the need for additional lead forming.

The disadvantage of the hot-bar soldering system is generally considered to be the still relatively high price (volume-dependent) given the low throughput volume.

5.2 Laser Soldering

Another alternative for the processing of fine-pitch components is laser soldering. The sequential soldering of individual leads potentially offers a high standard of quality under the following conditions:

- Fast and precise temperature measurement of solder joints

- Mechanical contact between connector lead and solder deposit must be ensured through a package-specific downholding element.

In contrast to hot-bar soldering, laser soldering does not appear to be sufficiently developed for mainstream use.

AUTOMATION IN PRINTED CIRCUIT BOARD PRODUCTION FOR THE ANALOGICAL AND PAN EUROPEAN (GSM) 900 MHZ CELLULAR RADIO SYSTEM: A SELECTION CRITERIA FOR SMT LINES.

G. FERRARI/M. MAGNELLI ITALTEL BUSR-II-T CASTELLETTO S. MILANESE

INTRODUCTION

In the highly competitive industry in which digital cellular and personal communication products are situated there are some key factors which are gaining an ever-incresing importance, such as:
- advanced production technologies
- flexibility of the production system
- total quality, in accordance with the new Business trend.

In particular, it is essential to adopt Surface Mounting Technology (SMT) because it can reduce the size of products and therefore ensure the compactness of the system.
Moreover, the SMT cause a reduction in production costs, since the advanced technological level reached allows the assembling of Quad Flat Pack (QFP) components in Fine Pitch Technique and the assembly of small outline components (SO) on the bottom side.
These components can now ensure the functional complexity required by the GSM product (microprocessors and Digital Signal Processors (DSP)).
At the same time, since the SMT is nowadays essential for almost all companies in this field, production flexibility becomes the real competitive advantage of a company over its competitors.
Our meaning of production flexibility:

- capability to change the production mix in a short time
- adaptability to new configurations or new products
- ability to reduce the interval between R&D and manufacturing start
- ability to react to changes of production volume

Whereas in the past, according to the "traditional" concept, the technical characteristics (Placement Rate, Accuracy, etc.) were those which determined the choice of the production line,nowadays due to new market needs and the consequent goal of flexibility, other factors become decisive (e.g. maintainability, possibility of reducting the set-up time, etc.).
This paper is intented to provide some considerations in the choice of SMT lines regarding the use of tools for production line design.
In the following text we describe the selection guidelines for the cases of traditional lines and newly-designed lines.

TRADITIONAL MANUFACTURING LINES

The traditional design parameters for SMT production line are aimed to the following aspects:

- machinery saturation
- local design on the machine level or, at most, on the jobshop level

In practice, when choosing an SMT line, the first parameter for analysis is that of compliance with production capacity requirements, as calculated with a formula of the following type:

$$CP = (Q \times C / Ha) \times K$$

CP = line production capacity (comp/h)
Q = expected production volume (pcb/year)
C = number of SMDs per PCB
Ha = available working hours per year
K = correction factor. It is a factor which takes into account organization inefficiencies, absenteeism, faults and repairs, maintenance, etc.

This means that the designing of the specific machinery (Pick and Place machine, screen printer, etc.) is carried out with the achievement production levels in mind, without takeing into the account the overall flow.
This leads to the overlooking of aspects related to higher costs caused by a large amount of Work In Process (WIP) and by the possibility of bottlenecks in other phases of the process flow, preventing the achievement of the global throughput target.

In addition to Production Capacity, the other aspect to be analyzed is the type of components which can be mounted.
Since in the digital communication sector the components are mainly microprocessor and DSPs, the relevant SMT production lines must have at least one module capable of mounting these components (QFP, TAB, etc.).

The above mentioned parameters in practice become a constraint by which the machinery available on the market are selected.
At this point the cost factor becomes the main comparison parameter, followed by other aspects such as:

- user friendly machine interface
- programming easiness
- machinery delivery time from the supplier
- placement accuracy

In accordance with the traditional concept of production lines, the investments are also evaluated with classical economical indexes such as NPV, IRR, Payback etc.

AVVANCED DESIGN RULES FOR SMT MANUFACTURING LINES

In the past, the notion of automation implicity meant a loss of flexibility in the production system.

Nowadays it is no convenient to automate manufacturing processes to the detriment of overall flexibility.

Automation is necessary to reduce variability in the production process.
It is a well-known fact that the intrinsic characteristics of the machinery are: uniform movements, regular cycle times and constant quality.

This implies the need to design new production lines by considering several new aspects which integrate the traditional ones.
These aspects are difficult to quantify in a cost benefits analysis and sometimes invalidate the effectiveness of economical indexes such as NPV, IRR etc.
These aspects are:

* MAINTAINABILITY. This means:

- Quickness and easiness of execution of day to day maintenance;

- Low frequency of ordinary maintenance actions. We report, as an example, the case of a speed placer machine which needs cleaning of the same part every five hours of work.
  This operation, which is not easy to carry out, may cause more stops in machine operation if it is not properly executed.

* RELIABILITY. Take into consideration:

- High Mean Time Between Failure (MTBF)

- Possibility of reducing the Mean Time To Repair (MTTR) thanks to the modularity of the basic elements (e.g. the positioning head of pick and place), which make it possible to easily change the faulty module and resume operation in a short time, with the repair being carried out off line.
  This also solves the problem of reliability of several heads on a line.

* SERVICE LEVEL. This refers to:

- Timely intervention by the supplier's technical service

- Short delays in finding the spare parts

- Supplier willingness to draw up a maintenance contract aimed at ensuring a constant level of machine performance and line availability, by means of preventive actions.

* REDUCTION OF SETUP TIMES

  It is this aspect which is most effective in achieving a reduction of the WIP and Lead Time (LT) in the production line

as a whole.
It is also the first step towards a possible reduction of lot size.
With traditional criteria, the lot size was chosen with the famous Economic Order Quantity (EOQ) formula, as a result of the minimization of total cost, obtained by adding the possession costs (interests on the locked-up capital) to the setup costs (cost for material picking and handling, cost for machine tooling and relevant check).

The reduction of the production lot implies the need to bring into practice new control methods before the assembly process to verify all the operations introduced by changing the setup, which may cause faults in the PCB functionability.
The availability of a number of machine positions for feeders to contain the full component mix of the whole equipment would make it possible to reduce the variability caused by the reduction of production lots.
These circumstances are difficult to provide with a product such as GSM, which is associated which relatively low volumes for the SMT and a very wide component range.

This leads to the need for having tools capable of designing an "optimal" setup in a short time.
In the following text we are going to illustrate one of these criteria.

HEURISTIC ALGORITHM

As we have seen, the goals of flexibility and cost reduction can be reached mainly through a reduction of the setup time and relevant operations by meaning the reduction of the handling of component feeders. It requires an analysis of PCBs mix. A heuristic algorithm has been developed for this purpose. Its logical steps are illustrated below.

1) ABC ANALYSIS OF COMPONENTS

Firstly It needs to obtain all the different SMD components from the "Bill of Material" of the equipment's boards.
By representing the quantities for each code on a chart, one can then identify the three allocation classes (A, B or C).
For the ABC diagram, see enclosure 1.

2) ANALYSIS OF COMPLEMENTARY CONDITIONS

There are initial conditions which may affect the algorithm's results.
These conditions may be:

- the need to contain in the same setup PCBs which belong to the same subset of the product

- for some groups of boards, constraints associated to the production flow following SMT operations.

Another hypothesis, aimed at achieving a high reliability of the algorithm's results, is the relatively low variability in the number of different component part numbers among the boards within their respective classes.
If this variability is actually high, it is convenient to remove the main reasons and consider the abnormal boards separately.

3) METHODS FOR REALIZING THE SETUP CRITERIA

The setup may be achieved by following two basic methods. The adoption of the ABC analysis method of component results.
These methods are :

a) Determination of the whole setup, starting from a basic setup, made up of A-class components.
   This method is preferable when A-class is the biggest.
   This makes it possible to complete the setup for a single board or at most for groups of boards by handling a small number of feeders.

b) Determination of the setup according to the criteria of associated boards with the largest number of common components.
   This is preferable when C-class prevails in the ABC analysis of components, because in this case the setup is expensive due to the high handling of feeders.
   This is the case with the GSM product.

After defining the criteria which associates the pcbs with the largest number of common components as the reference criteria, we proceed as follows:

4) DETERMINATION OF THE REQUIRED FEEDERS POSITIONS

A program produces a list of all the component part numbers, with an indication of their respective shapes.
Each component shape is associated with a number representing the relevant required feeder area ; for example, chip 1206 requires 1 feeder position, QFP requires 7 feeder positions, etc.

5) ABC DIAGRAM FOR THE BOARDS

Let us carry out an ABC diagram with the quantity of different component part numbers for each board.
The three groups created must be homogeneous in the quantity of boards contained.
In the GSM case, see enclosure 2.

6) DETERMINATION OF THE REQUIRED SETUP NUMBER

we define:

Mnec = number of machine feeders required
Mava = number of feeders available on the machine

The relationship:

N = Mnec / Mava

rounded off to the higher integer, provides the minimum number of setups needed to start the algorithm.
If N turns out to be insufficient to allocate all the boards, the algorithm must be repeated with N increased by 1.

7) DETERMINATION OF "A" CLASS BOARDS TO BE ASSOCIATED IN THE FIRST SETUP

The number "n" of A-class boards are divided by N:

R = n / N

R, rounded off to the higher integer, is the number of A class boards that we must associate to build the setup.

8) SETUPS ACHIEVING AND SETUP TREE DRAWING

If R is greater then 1, a number of R A-class boards must be combined to be the first setup.
To do this, we start by associating the "n" boards by couples.
For each combination of two boards we determine the quantity of common components part numbers.
The two boards having the largest number of common codes will be the base for the next iteration, which will still concern A-class boards until a number of R boards are associated.
The following iteration,at this time, is made with B-class boards.
The process is repeated again with C-class boards.
If, during the check with the number of available feeder position there is a possibility of inserting more boards, the process will be repeated starting from B-class boards.
The setups are obtained by repeating the above mentioned process.
With this algorithm it is possible to optimize the use of the production line and to provide setup operations in a short time, thus improving also the industrialization process for a new product.
As soon as the "bill of material" for the boards are available, it is possible to have immediate feedback about the following aspects:

- needs which may arise from revising the component plan to reduce the number of setups , according with the "design to cost" concept
- indications about the opportunity of reconfiguring the lines, or planning new investments for new lines.

In this case the quickness of the result provides more time to evaluate investiments for advanced equipment.

CONCLUSIONS

In conclusion , we wish to mention the use of simulation techniques to measure parameters such as WIP and LT, which highlight the overall flexibility target.
In fact, these tecniques and an adequate line model allow us to check some parameters such as the lot size variation.
These tools also make it possible to take into consideration design alternatives which have not been covered in this paper, such as the parallel line designed.

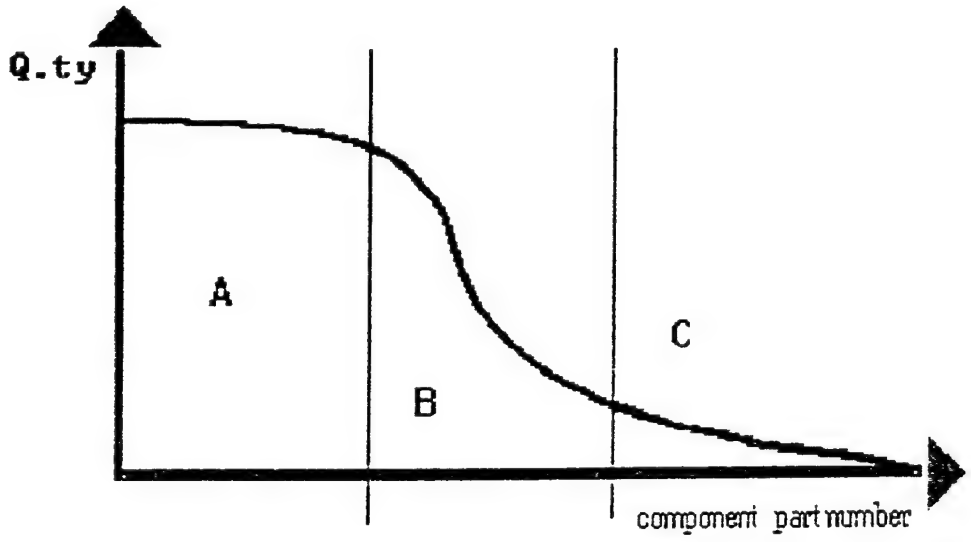
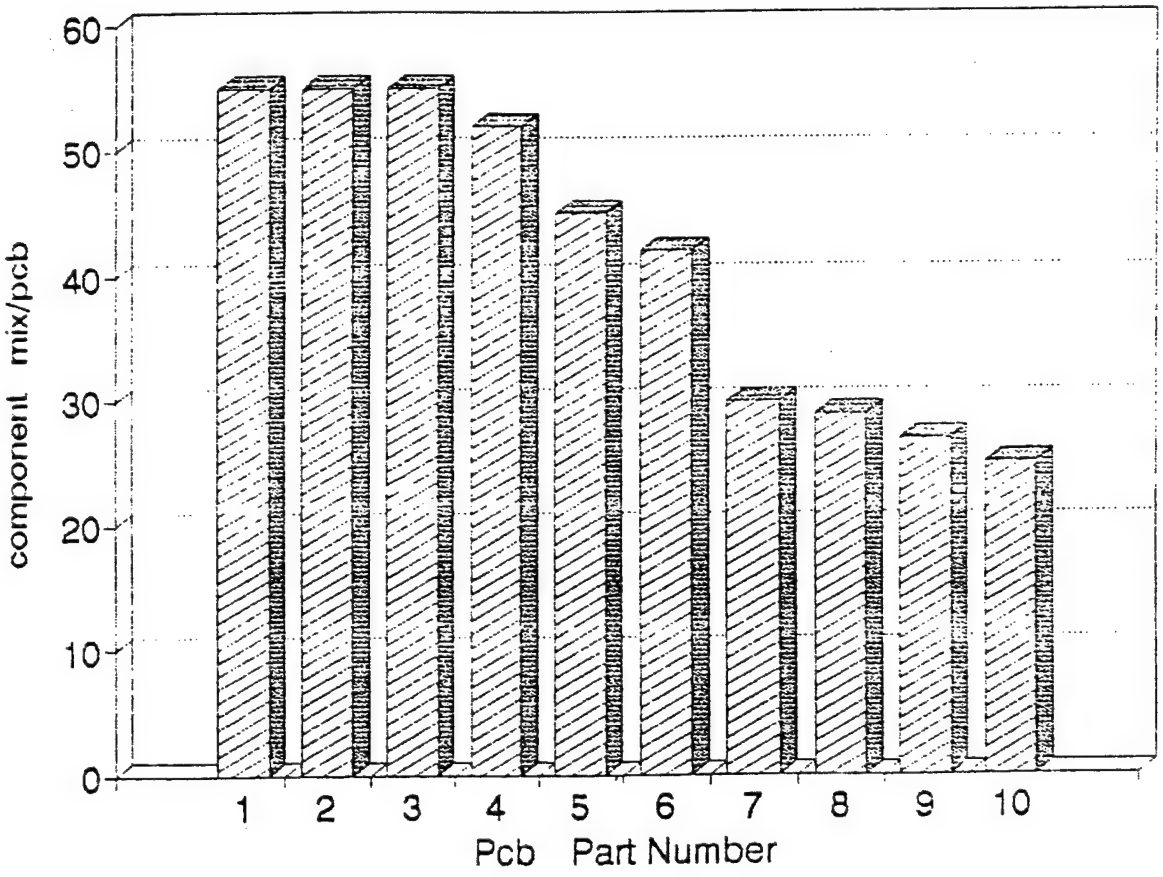


FIG.1

FIG.2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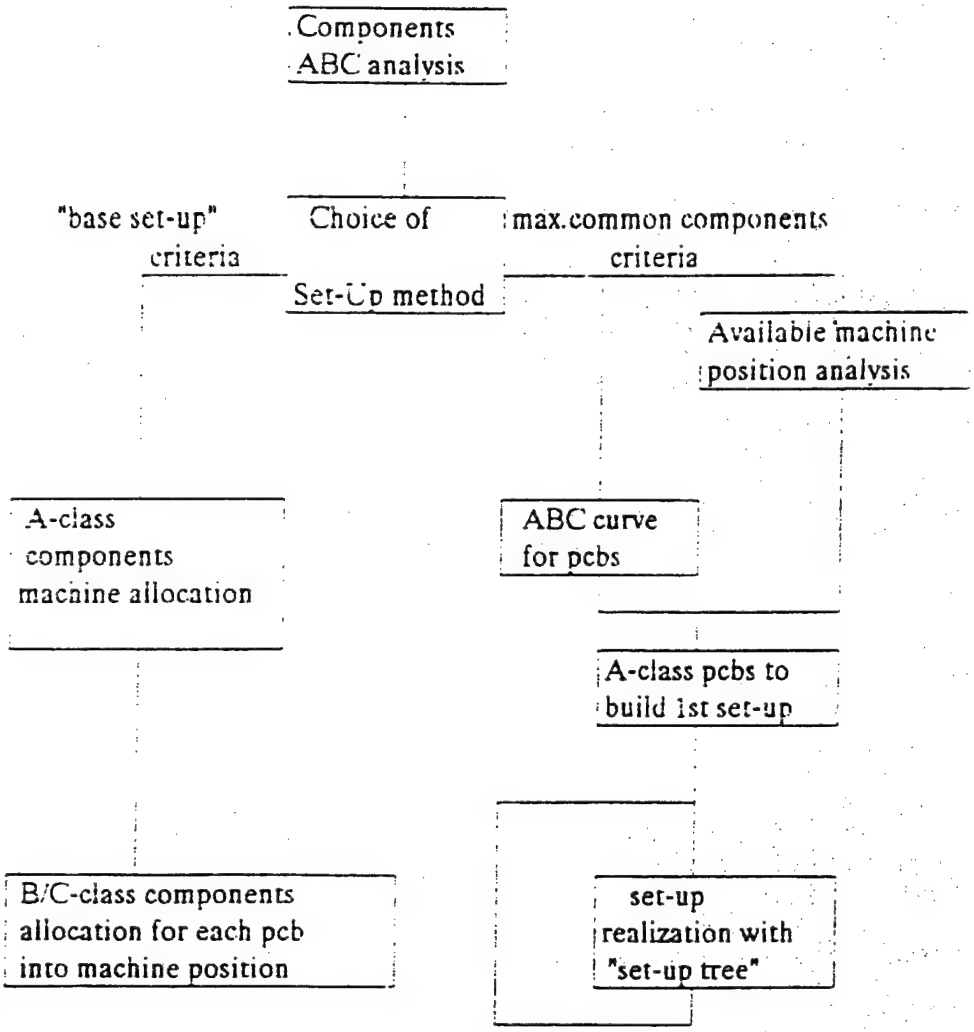
HEURISTIC ALGORITHM



TEST AND MEASUREMENT SOLUTIONS FOR DIGITAL MOBILE RADIO

by David Picken, B.Sc.(Hons), Rohde & Schwarz, Munich, Germany

The novel technologies employed in the pan-European digital cellular radio network (GSM) call for test and measurement functions not available in conventional instruments.

This contribution presents the most significant new features of a family of test and measurement equipment conceived especially for GSM applications. It describe the major differences between conventional radiotelephony and the rising generation of digital networks, of which GSM is a particularly prominent example.

1. Identifying the Challenges

1.1 The New Aspects in GSM

Although in the early days of GSM equipment development engineers were obliged to make use of existing conventional measuring instruments, companies such as Rohde & Schwarz took up the challenge of introducing special instruments for the GSM community at a very early stage. In modern digital radio networks there are many novel testing requirements which cannot be met by conventional measuring instruments such as signal generators, power meters and spectrum analyzers.

Among the new features described by the 5000 or so pages of GSM specifications, those most relevant to the testing of mobiles and base station equipment are:

* the transmitted information is fully digitised and thus time-discrete.

* advanced digital modulation techniques influence both the phase and amplitude of the radio-frequency carrier signal in a defined way at every instant in time.

* the transmission of data blocks (telegrams) at specified moments in time, known as time slots, is a further characteristic of GSM and other systems using the TDMA approach.

* Time division multiplexing presupposes accurate synchronisation between the radio stations in the network. In a measurement context, this implies synchronisation of test equipment to the data exchange mechanism within the radio network.

* For adequate resolution along the time axis, sampling rates are called for several times higher than the effective symbol transmission speed.

* A further challenge to the instrument designer is presented by the amplitude range of the signals on the radio path. The specifications call for 70 dB between the "maximum-power" and "off" conditions of a transmitter.

* the use of changing carrier frequencies, even in a relatively slow frequency-hopping scheme, also call for new measurement functions in signal generators and analyzers in order to simulate or follow the known hopping sequence.

* complex coding and interleaving schemes for secure data transmission must be simulated and analyzed, requiring powerful processors and extensive memory

* the introduction of predictive speech coding will to all effects spell the end of conventional audio signal measurements.

1.2 Features of the GSM Network in Review

Structure. While the network structure of GSM is similar to that of existing cellular systems, it has been designed from the start to accommodate data transmission. Thus connection is possible either to the public phone network or the ISDN and other data networks. Data services may use internal features of the mobile (short messages on an alphanumeric display) or require external equipment such as a facsimile machine.

Air interface. The air interface between the base stations and the mobiles is summarized below:

GSM SYSTEM FEATURES	
Frequency ranges	
Base station receiver	890-915 MHz
Base station transmitter	935-960 MHz
RF carrier spacing	200 kHz
Duplex	
Duplex frequency offset	45 MHz
Timing offset	3 timeslots between TX and Rx with timing advance
Timing	
Bit duration	3.692 μs
Timeslot duration	576.9 μs
Frame length	4.615 ms, 8 timeslots per frame
Digital modulation	GMSK (Gauss Minimum Shift Keying)

The duration of each data bit is 3.69 microseconds, giving a data transmission rate of 270.833 kbit/s.

All transmissions are organised into timeslots and frames (see figure 1). Eight timeslots (bursts) of 156 1/4 bits in length make up each frame.

The training sequence is a fixed bit pattern used for synchronisation and as a reference for the equalizer filter in the receiver which has the task of compensating for multipath distortions.

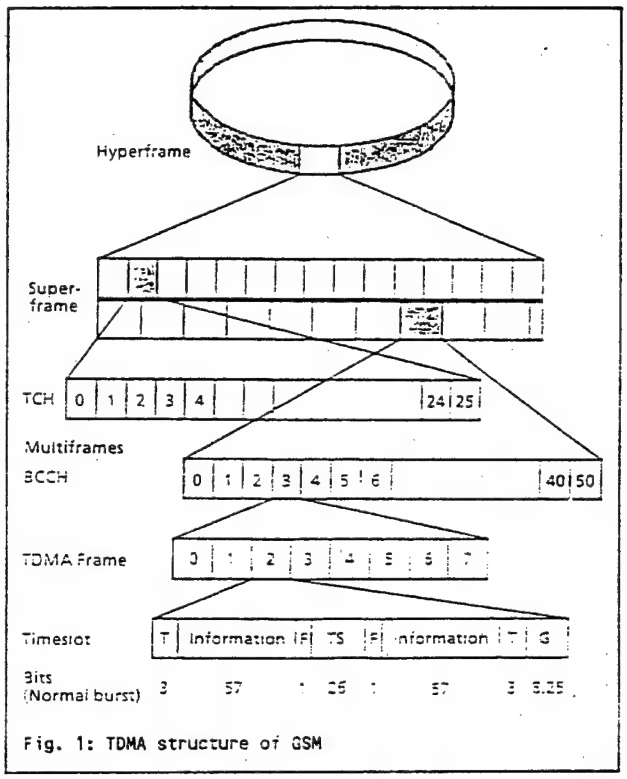


Fig. 1: TDMA structure of GSM

To improve the overall performance of the system, the useful information is not only coded using forward-error-correction techniques but also distributed among a number of timeslots (interleaving). These timeslots, in turn, will be transmitted at different frequencies according to a frequency-hopping sequence.

Multiplexing. GSM transmission uses a combination of both frequency division multiplex and time division multiplex.

GSM speaks of several channel types:

The radio-frequency carriers are designated by their absolute RF channel numbers.

The transmission pipeline, however, is made up in general of one time slot per frame (a full-rate channel). This pipeline is referred to in GSM as a physical channel, and is defined by slot number, frame number and a sequence of RF channels over which the signal hops.

The third channel type has been called the logical channel, being a reference to the function performed by a particular stream of bits.

The GSM logical channels may then be categorized as:

* Traffic channels - used to carry digitized speech or other data. The traffic channels are further classified by the speed of transmission possible.

* Control channels - used for signalling and synchronisation of the mobiles. Control channels are further divided into:

- Broadcast channels - used for frequency correction, frame synchronisation and for identifying the base stations

- Common control channels - used for calling (paging) mobiles or providing mobiles with access to the network

- Dedicated control channels - used, in general, together with traffic channels for management tasks.

Speech coding. Since the conventional method of digitizing speech in telephony (PCM) requires a transmission rate of 64 kbit/s for adequate quality, ways were sought of reducing this bit rate to below 16 kbit/s to allow efficient use of the radio spectrum.

The predictive coder chosen reduces the bit rate to 13 kbit/s (260 bits for each speech sample of 20 ms duration). After error-protection coding, each speech channel requires 22.8 kbit/s at RF.

For added protection, the bits of each speech sample are distributed over two RF time slots by a process called diagonal interleaving.

For the future, it is planned to introduce speech channels working at half the rate (11.4 kbit/s) in order to increase the system capacity, making use of current advances in vocoder technology.

2. Measurement Requirements and Solutions

2.1 Measurements on GSM Receivers

Signal generation. Modern signal generators are required to convert a prepared bitstream (the signalling) into a correctly modulated RF carrier. Conventional generators are unsuited to this task because, as a rule, they do not permit direct control of the carrier phase in the way the GMSK technique requires. Generation of such signals is the domain of instruments using I/Q modulation. Digital signal processors will derive the complex I and Q phase modulation signals from the bitstream information.

The frequency hopping and time multiplex features of the GSM network also make fast switching of both frequency and amplitude of the signal generator necessary in order to simulate the typical signal bursts which occur in practice.

Figure 2 shows the principle of modern signal generators meeting the requirements described. Once such unit is the signal generator SMHU 58. With its I/Q modulator it provides suitable test signals, particularly as a high-purity interfering source in critical blocking and adjacent-channel rejection measurements.

Fading simulators, used to reproduce the multipath and doppler fade effects of the radio channel, gain in importance in a fast digital network such as GSM. These complex and costly units will, however be restricted to research and type-approval work.

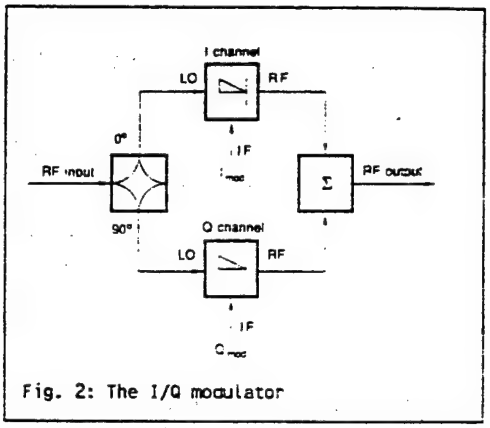


Fig. 2: The I/Q modulator

As in conventional radio systems, the receiver sensitivity is one of the critical parameters. Since, as a rule, measurement directly behind the demodulator will not be practicable, the GSM specification writers have devised a loop-back technique in which the radio itself provides information on the quality of the received signal. The results are retransmitted by the mobile to the test equipment as an RF signal. The instrument analyses this looped signal in order to compute the receiver sensitivity, expressed as a bit error rate (BER) or as a frame erasure rate (FER).

2.2 Measurements on Transmitters

Conventional power meters and modulation analyzers work only with steady-state signals. They are thus of little use in the analysis of bursty signals such as the TDMA timeslots of GSM.

The only viable approach to analysis of such signals is to sample the RF signal or the down-converted I/Q equivalents at a high rate. Since the I/Q signals represent both the amplitude and the phase of the original RF signal, they may be used for many different forms of analysis. The sampled values can be written into memory for analysis in later processing steps to give:

* demodulated phase vs. time
* detected amplitude (power ramp) vs. time
* phase noise (computed as the difference between the measured and theoretical phase trajectories)
* demodulated frequency vs. time

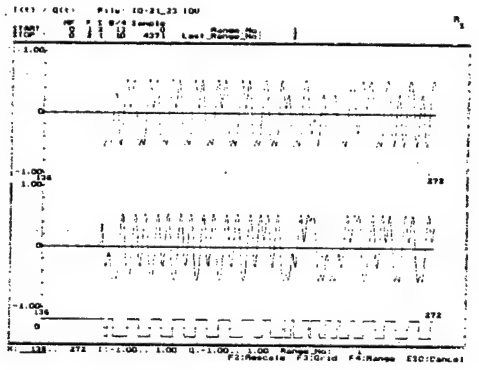


Fig. 3a: I/Q samples plotted vs. time

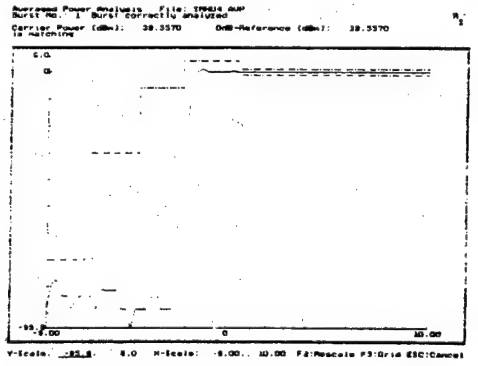


Fig. 3b: After conversion to power values, the samples are compared with the GSM power-time template. Here the leading edge is shown using the zoom function.

Figure 3 shows examples of such measurements on an RF carrier signal.

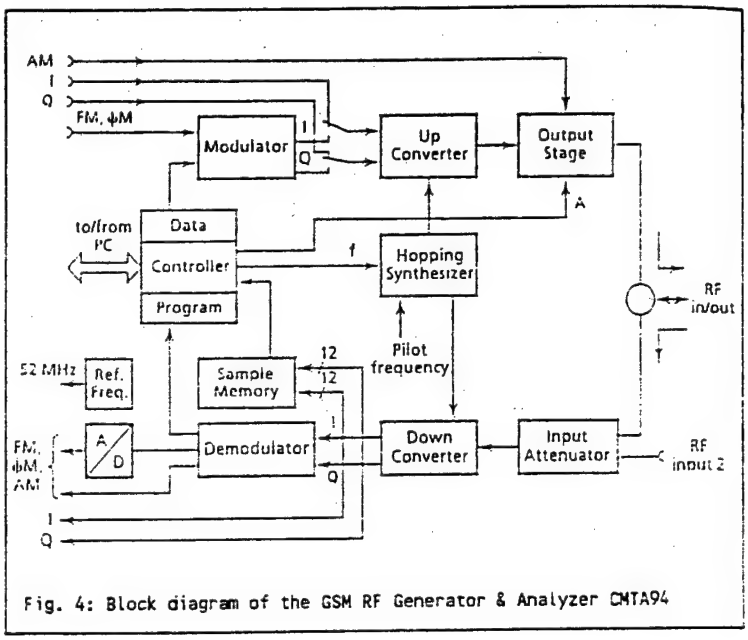


Fig. 4: Block diagram of the GSM RF Generator & Analyzer CMTA94

The GSM Radiocommunication Analyzer CMTA 94 was the world's first testing tool to combine a signal generator and a signal analyzer with GSM-specific features (see figure 4).

The signal-generator section allows free definition of GSM bitstreams, ensures correct modulation using GMSK as specified by GSM and packages the modulated data into bursts in accordance with GSM's TDMA structure. Frequency hopping simulation is also possible, thanks to the synthesizer's 500-microsecond switching time.

The analyzer part of the instrument, which may be used in a duplex mode simultaneously with the generator, captures the RF output of the radio transmitter by sampling the I and Q components of the carrier.

In a comfortable system of menus, the user can rapidly present these results as graphs or tables showing the I and Q voltages or the equivalent power, phase-modulation or frequency-modulation traces versus time. The demodulated bitstream is also available as a realtime signal or as a table of results. Complex high-speed algorithms running in a digital signal processor convert these raw data into the GSM-specific power-ramp and phase trajectory curves.

2.3 Signalling Measurements

Besides the classical RF aspects, public radio networks such as GSM also involve complex signalling schemes which have to be handled by the test equipment. There has been a high demand for flexibility, since the standards were still going through their final stages of consolidation while the radio equipment was being developed.

Protocol test equipment for radio networks, such as the family of GSM Radiocommunication Test Sets CRTS (figure 5), are distinguished from their equivalents in the world of wire networks by the very powerful combination of RF and signalling features they provide. Like the network itself, such signalling testers are structured around the Open Systems Interconnection (OSI) model for the lower three protocol layers on the radio interface U_m. A modular design concept permits different configurations of microprocessors, digital signal processors, special RF hardware and software tools, matching the wide spectrum of functions required in the various applications:

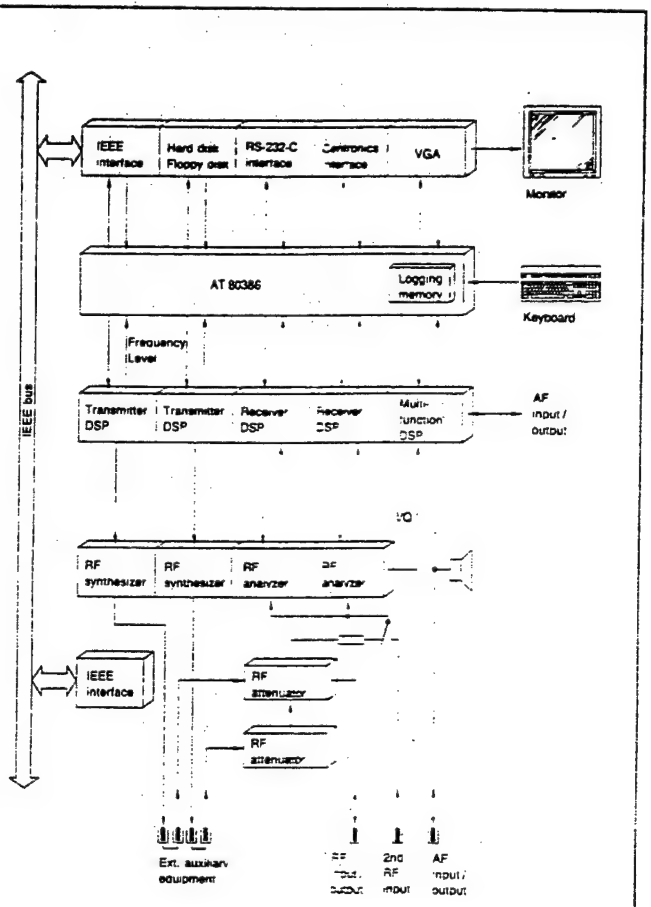


Fig. 5: Block diagram of GSM Signalling Test Sets CRTS

* GSM message handling. A powerful software tool - called the message editor - eases the task of defining specific messages. Thanks to the use of an intelligent data base, the user is saved much of the trouble of referring to the GSM specifications.

* Layer 3 (network) signalling sequences for simulation of call connection and management procedures can be user-specified.

* Layer 2 (data exchange) mechanisms. Besides automated (correct) data link operation, error implantation is also needed for simulation of practical transmission problems.

* Layer 1 coding functions. Binary data are coded and interleaved for protection against transmission errors. Ciphering further ensures confidentiality of the user traffic.

* Logging of signalling activities. Due to the speed and complexity of the signalling process, the only way to locate protocol trouble spots is to record interface activity in a large memory. Once again, it is the task of comfortable software to present the logged protocol in an understandable fashion for rapid and meaningful analysis (figure 6).

* Layer 1 physical transmission functions. Modulation and demodulation, frequency hopping and power ramping all have to be simulated and analyzed in the test equipment.

* Speech coding/decoding. The final test of a GSM radio comes when the voice connection is established. Vocoder functions in the test set ensure that true-to-life speech tests can be made on the finished radio before delivery to the customer.

* GSM-specific RF measurements. Receiver sensitivity based on BER tests, transmitter power-ramping and phase-noise performance: these tests are best handled by high-speed digital signal processors in order to achieve accurate results in acceptable times.

* Synchronization facilities. With its timebase of 13 MHz and its complex TDMA structure of frames and multiframes, the GSM network poses some special problems in the synchronization of instrumentation. New equipment provides GSM-specific timing inputs/outputs, while powerful accessories also permit existing instruments with the usual 10-MHz sync to be tied into GSM test setups.

File Edit

Log - Mnemonic	Base Station	Buffer Channel	Log Frame Number
TX Paging Req Type 1	2	PCH	9307
RX DL-RA-Ind	2	RACH	9318
TX Immediate Assignment	2	AGCH	9362
RX Measurement Report	2	SACCH	9434
RX Paging Response	2	SDCCH	9453
TX System Info Type 5	2	SACCH	9521
RX Measurement Report	2	SACCH	9536
TX CC Setup	2	SDCCH	9540
RX Call Confirmed	2	SDCCH	9606
TX System Info Type 6	2	SACCH	9623
RX Measurement Report	2	SACCH	9638
RX Alerting	2	SDCCH	9657
TX System Info Type 5	2	SACCH	9725
RX Measurement Report	2	SACCH	9740
TX System Info Type 6	2	SACCH	9827
RX Measurement Report	2	SACCH	9842
TX System Info Type 5	2	SACCH	9929
RX Measurement Report	2	SACCH	9944
TX System Info Type 6	2	SACCH	10031
RX Measurement Report	2	SACCH	10046

F1-Help F2-Save F3-Load F4-Expand F5-Contract F8-Buffer/Log F10-Menu

Fig. 6: Example of a signalling log recorded by the CRTS

In the light of the high complexity of the GSM signalling protocols, users rely to a large extent on the software of the instruments to reduce the burden on testing staff. The CRTS

instrument family addresses this need by providing a comfortable message editor environment for the creation and analysis of all GSM layer 3 messages. By decoding the message content into easily understood text, the message editor automatically takes care of the requirements of the GSM 4.xx Series recommendations.

Models of the CRTS are available for exercising mobile terminals or base stations.

3. Applications of Test & Measurement Equipment

3.1 Design and Type Approval

Flexibility and depth of testing are common to both of these application areas. Whereas the design work is often a matter of extreme secrecy, type approval is only possible by presenting the new product to the postal authorities or an accredited test house. Type approval is particularly important for the end-user equipment, the GSM mobile station. The exhaustive tests performed during the type approval procedure have been designed for various reasons: proof of correct operation within the network; electromagnetic compatiblity (EMC); and, of course, conformance to minimum transmission quality standards. The complete type approval test system, covering all these measurement aspects, is known as the GSM System Simulator (figure 7).

For those involved with the preparation of equipment for type approval testing, or where there is a need for interim type approval testing, an alternative is available in the shape of the Interim Type Approval (ITA) System based on standard instruments.

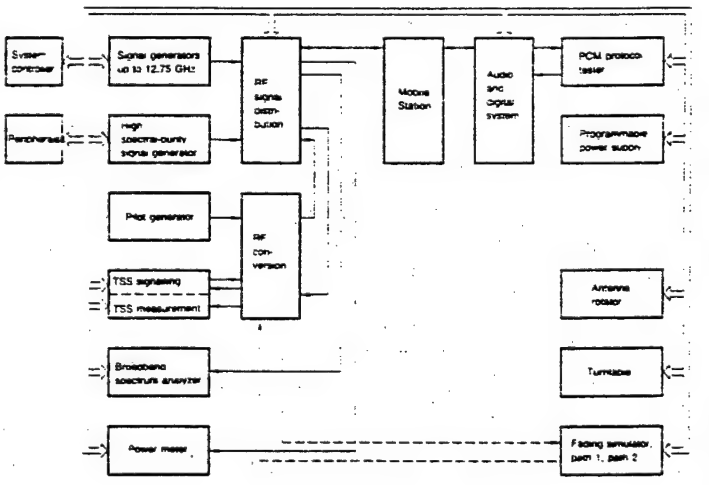


Fig. 7: Block diagram of the R&S System Simulator for type approval testing of GSM mobiles

3.2 Manufacturing

More than anywhere else in the industry, high testing speed and low investement and operating costs are essential features for instruments used in mass production. With production gearing up to several hundred radios daily, test times are getting down to just a few minutes per telephone. The GSM-MS Production Tester CRTS 12 has been conceived with this special market in mind. Besides measuring all the standard parameters

such as Tx power, frequency, modulation and Rx sensitivity, it also handles the signalling sequences needed to simulate a GSM base station and can run fully automated tests to guarantee the continuing high quality of the radiotelephones.

3.3 Installation and Service

Mobility, ease of operation and flexible test programs are the primary requirements for field testing. Integrated testers, such as the CMTA 94, are already proving invaluable for the installation of base site equipment. These new RF testers team up with existing PCM protocol analyzers to put the GSM base station through its paces.

The high level of integration of upcoming GSM mobiles will reduce servicing up front at the dealer to board or module exchange. The real repair work will be concentrated in centres of expertise, where a large market can be expected for a second generation of GSM test sets.

3.4 Coverage Measurements

Coverage measurements are needed to prove the results obtained by mathematical modelling and to ensure the high grade of service expected by the paying customers. Of particular significance are the test receivers used for investigation of propagation conditions. Measurement drives through different types of terrain take up a lot of time and can only be carried out on a meaningful scale if automatic test equipment is available. Modern fieldstrength measuring systems are designed especially for digital networks. They combine high measurement rates, efficient positioning techniques and statistical analysis software. The results may be readily linked to existing cartographic data to provide essential information for site selection and coverage planning in the targetted service areas.

Beyond the simple measurement of fieldstrength, digital networks such as GSM also call for the evaluation of the received signal quality as a bit error rate (BER). In addition to the logical detection of bit errors on a known transmitted signal, researchers often call for more generalized techniques of describing the radio link. One such method is "channel sounding", in which the complex impulse response of the path, with its multiple reflections and fading effects, is determined.

Advanced Signal Processing Technologies in GSM

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I. Introduction.

Cellular telephony technologies are receiving rampant attention worldwide. Public acceptance is burgeoning into consumer product-like growth. Standards are being developed all around the world, resulting in a proliferation of legislative, technical and algorithmic development work. Manufacturers everywhere are striving to develop cost-effective product which will enable the industry to continue, and in fact increase, its fast growth rate.

What is required to realize the true market potential of cellular technologies? Does the competition between international standards help or hinder potential growth and market acceptance? To truly experience growth and evolution into a consumer market, cellular products must meet the three fundamental commercial drivers: Price/performance, price/performance, and price/performance.

This leads to the question of whether overall market needs match with fundamental semiconductor business concerns. Price of silicon products vs. development costs, risks in market development, market share, etc. requires constant re-evaluation. Given the multiple worldwide cellular markets, is it more reasonable for a semiconductor supplier to develop multiple optimized silicon solutions for each international standard, or to develop a more universal offering tailored to generic industry needs?

Manufacturers continue to specify additional value-added functions and features above and beyond the basic cellular product. What is the economic impact of these needs on the semiconductor supplier? How can they be implemented cost effectively?

AT&T Microelectronics has long been active in silicon product developments for cellular systems. Today's offerings, future evolution and new products, are based on matching AT&T capabilities to market needs within general semiconductor business guidelines.

Products have been developed to provide the high performance demanded, while allowing for easy modification and adaptability to handle alternative industry standards as well as manufacturer-specific value-added functionality. By maintaining a balance between specific system needs and real world economic constraints, AT&T can provide products with best price performance trade-offs for cellular system manufacturers.

For GSM, AT&T has developed a 2 chip offering for the RF/IF, up/down conversion functions using Bipolar technologies. Close work with strategic partners has led to the development of a single chip baseband converter IC for signal conversion as well as control functions. Core DSP technology is used to develop the software configurable, high performance, low-power CMOS, fully static digital processor chips for all baseband functions. AT&T ASIC technology is also available for further custom control products. All products are available now.

This paper reviews market trends and needs as well as semiconductor industry constraints. We present AT&T Microelectronics' approach which best benefits all involved in cellular product development.

II. Market Overview.

There are many market variables which cannot be definitively answered. This leaves open numerous questions about market size and potential due to market acceptance, competing standards, market shares, etc. We briefly review some of the key questions which we feel impacts our ability to properly define and provide timely semiconductor products for Digital Cellular applications.

Current market forecasts (source: Mobile Europe) indicate continued growth in Europe for Analog Cellular Systems until about 1993-94. By 1995-96, it is expected that GSM Digital Cellular Systems will begin to dominate the mar-

ket and analog share to begin declining.

Today, several European countries, such as Spain, have only recently introduced Analog Cellular services. How quickly can these countries be expected to change over to Digital GSM? How long before their 'return-on-investment' criteria are satisfactorily fulfilled?

Analog service providers have invested significant amounts into network development. Analog terminals manufacturing has matured and profits are being reaped. Just how soon will the analog services allow GSM to gain market share? What kinds of competition can be expected from analog?

Subscriber estimates for the year 2000 consistently fall in the range of 15-25M GSM users. Will subscriber interest really blossom to this level of user density given the choices between different services and technologies such as CT2, DECT, and PCN, and the associated price/performance tradeoffs?

Current analog terminal suppliers have relatively low market shares. This is due to the continuously growing supply of manufacturers. Of the European manufacturers, none now holds more than a 12% total market share in the European market. And market shares are continuing to erode due to increased competition.

Will GSM suppliers face the same scenario? It can be expected that as GSM matures and market acceptance and proliferation increases, more manufacturers will strive to carve out market shares. Therefore, it can be expected that ultimately, no single manufacturer will have more than 10-15% share of the market.

What are the effects of these market dynamics on semiconductor suppliers and their internal development plans for integrated circuit manufacturing?

There is competition still from Analog Cellular. There is overlap and competitiveness from competing standards. Market growth may not be as rapid as forecast due to price/performance trade-offs. Manufacturers may be facing limited market share opportunities. The question then is *not what* a semiconductor supplier might supply for terminal manufacturers, but *when* higher levels of integration should be pursued for manufacturers.

III. Semiconductor Industry Concerns.

In the semiconductor business, volume is ultimately the driver. However, when supplying into a consumer-type of product, there are some issues and constraints which must be weighed out.

Ideally, semiconductor manufacturers strive for the highest yield performance possible, irregardless of chip complexity. This is pursued using advanced design tools and intelligent system partitioning and chip configuration. However, there are trade-offs between yield, packaging, and testing costs. The key to achieving the best total system price/performance is system partitioning. Simply integrating as much as possible onto one die may not be cost effective.

Larger, more complex circuits generally require more expensive packaging. This impacts pin count, package type and assembly costs. As pinouts reach 200 or more, costs begin to rapidly, non-linearly increase.

In order to minimize total system costs, there must be a strong relationship between the system architects and the silicon manufacturers to best partition a large complex system into units which are ideally sized to provide an optimally priced solution.

Investments by silicon manufacturers must also be made for time and labor in design, layout, simulation, testing, etc. Clearly, these costs increase with device and system complexity. Furthermore, close interaction on the systems partitioning and architecting require more than just silicon design knowledge and tap into other engineering talents.

Therefore, it is imperative that a semiconductor supplier carefully review the market conditions and system design issues for a consumer-oriented application before investing in development of 'standard' chipset products.

IV. Market Evolution.

Development and evolution of the GSM and PCN markets can be rationalized into three phases. In Phase I, the system is introduced, new services are ramped up, new products and technologies are being tested and proven, and market reactions and acceptance are being measured. Clearly this is the current status of GSM.

Phase II can be considered the industry competition phase. A number of initial players may back away or leave the arena. New players will

target their own market shares. The network will be expanding and market acceptance will be growing. Services will improve with new features being offered.

Phase III would be the commodity market mode. Here, GSM and PCN terminals would be readily available and consumer priced, services would be available for a variety of needs, and most importantly, high volume sales would be experienced.

Each Phase imposes different driver impetus to the different players. For the purposes of this paper, we examine the conditions of each Phase in the market, on end equipment manufacturers, and on semiconductor suppliers.

In Phase I, the initial market would be the high end professional or business users. These users have different needs and demands than the typical consumer. They are highly mobile, probably travel often, and require constant accessibility and the ability to spontaneously contact others.

The system and terminal manufacturers are producing 1st generation product. Initially, these may even be demo or product prototype models. Only basic functionality would be provided. Offerings would not necessarily be optimized in terms of power, size, weight, etc. because a 'proof-of-concept' is still being conducted.

Semiconductor suppliers would prefer to provide standard products because of lower risk, lower investment, and to provide a more flexible solution for the manufacturers to do testing and make modifications.

Phase I can be described as the *Capability Demonstration Phase.*

The market in Phase II will be larger - reaching into smaller businesses, achieving status symbol recognition, and possibly even gaining some consumer (home) clients. However, there would be confusion in the market due to the competing types of systems - primarily between Digital Cordless and Mobile. Therefore, there would be specific marketing and promotion plans being implemented by service providers and terminal manufacturers.

The terminal manufacturers would be striving to increase market share by differentiating their products from competitors. This could be in size, ergonomics, weight, battery lifetime, features, performance, etc... Associated with these differentiators, there would have to be promotion (sales and marketing) plans. A key to achieving this product differentiation will be the way software is integrated with hardware.

This means that semiconductor suppliers must work closely with terminal manufacturers to define architectural partitioning and software and hardware interdependencies. 2nd generation silicon products would most likely be evolved from 1st generation products. Development of new optimized standard products may be considered, but market share opportunity vs. development costs is still a debatable issue.

Phase II can be described as the *Product Differentiation Phase.*

We now reach the consumer/commodity market phase. Here, GSM and PCN terminals are abundantly available and priced for the average consumer. This would be similar to stereo, TV and other mid/high-end electronics equipment. The drivers will be price and performance. Certainly product differentiation will exist, but one would expect a variety of grades of equipment available on the market.

Manufacturers would be leveraging their distribution/retail skills and manufacturing technologies. The internals of the products would be highly integrated and well defined to bring costs down the price curve. New market share leaders will emerge due to superior retailing and lower manufacturing costs.

Semiconductor suppliers would be expected to provide standard chipset offerings - and rightly so because finally, the market demand (volume sales) would warrant the investments expended to develop these solutions. Semiconductor manufacturers also would be leveraging their integration and manufacturing skills.

Phase III could be termed the *Manufacturing Phase.*

Having defined the market phases, the key question is to define the timeframes during which they will occur. Proper product development and introduction timing is the key to timely recovery of investment dollars.

V. AT&T Approach.

AT&T has been very active in GSM developments and closely aligned with key manufacturers. These relationships have helped AT&T to define their interpretation of *when* the market will evolve through each Phase.

This has led to AT&T's current product portfolio and future product development plans. Clearly, given the current status of GSM implementation, AT&T's offering of standard programmable MOS products for testability and flexibility can be easily understood. The AT&T RF/IF front-end products are by necessity 'hardwired' devices. Specifications and performance of the RF/IF front-end are clearly defined by the standards.

As manufacturers move into design of Phase II products, AT&T is offering MOS products with programmable cores and hardware acceleration features. This approach enables manufacturers to achieve better price/performance trade-offs as well as the ability to develop market competitive products by coding-in feature differentiations.

AT&T believes that Phase III will not occur until end-1995 or 1996. Phase III will also be much more focused on PCN products than GSM mobiles. For manufacturers to have products available in 1996, new silicon design and development must be underway in 1992 or early 1993. AT&T is further developing customer alliances for defining silicon products suitable for consumer cellular applications.

VI. AT&T Products for GSM.

AT&T has developed RF/IF front-end chips using our Bipolar processes. A baseband converter product has been developed for digitizing (sampling) the I and Q complex baseband signals. For digital processing, AT&T has developed a 'Signal Coding' Digital Signal Processor (DSP) to handle Equalization (EQ) and Channel Coding (CC) functions.

For the interface to the user, two options are provided. AT&T has developed an integrated voiceband codec + DSP for handling the Speech Coding (SC) function and other desired user interface functions. An alternative would be to use a separate voiceband Codec and a fixed-point DSP such as the Signal Coding DSP.

RF/IF Products.

Two chips, the RF1 and UB1318, are standard catalog offerings which together form a complete Rx/Tx chipset solution. Both were designed specifically for GSM application.

AT&T has taken a cell library approach to designing the front-end chips. Numerous analog cells have been designed to meet GSM specifications. These include cells such as:

- Low-distortion Preamp
- Receive Buffer
- Balanced RF-to-IF Mixer
- IF Buffer
- RF Quadrature Mixer
- IF Quadrature Mixer
- IF-to-RF Mixer
- RF Output Buffer.

This approach offers flexibility of design so that manufacturers are able to configure their own functional blocks. These cells also provide further custom opportunities.

AT&T also offers a customizable building block approach at a functional level (as opposed to the low level analog cells). Designers may customize their RF/IF architecture by selecting from building block ICs such as:

- Modulator and IF Amplifier (30 dB)
- Amplifier and Mixer (130 MHz)
- RF/IF Mixer and Amplifier
- Direct Up Transmitter (Modulator and Amplifier)
- IF/RF Mixer
- Baseband-to-IF Modulator
- Demodulator (130 MHz)
- High Frequency Differential-to-Single Ended Converter
- High Frequency Single Ended-to-Differential Converter

Both current standard products have been developed with operational considerations in mind. Both have very low power consumption and sleep modes for longer standby battery life. Gain control in the IF stage is digitally programmable from 6-75 dB. A Low-Noise-Amplifier (LNA) is provided on-chip. Both are packaged in 28-pin SOG packages and are competitively priced.

AT&T has also recently announced a variation on the UB1318 IF chip - the UB1468. This device has better phase error performance and lower offsets than the UB1318. However, this device requires an IF oscillator frequency which is 4 times higher than required by the UB1318.

The UB1468 is just the first example of how AT&T will continue to evolve and improve RF and IF chip offerings. These products, as well as the analog cell and building block approaches provides system designers with a clear technology evolution path.

For PCN applications, another aspect of semiconductor manufacturing becomes critical. This is packaging. For consumer markets, low cost is required. At 1.8-1.9 GHz, packaging techno-

logy innovations are required to satisfy the technical issues (such as offsets, lowering lead inductance, ...) as well as the commercial issues (such as small outline, plastic, ...).

MOS Products.

AT&T has focussed it's activities out of the Digital Signal Processing (DSP) Business Unit. This group has the expertise and understanding on the high complexity processing algorithms required in GSM and PCN systems. However, AT&T also offers ASIC standard cell design capability for custom developments as well as programmable DSP products. Key features of AT&T's general MOS process are:

- 0.9µ (drawn) 2-level-metal CMOS
- 3.3v. operation
- Fully static designs
- Migration paths between FPGA, GA and Standard Cell designs

ASIC technology is ideally useful for developing custom glue-logic ICs. AT&T's ASIC cell library approach has been used to develop custom user interface controllers for handling display interfaces, parameter handover, etc. Cells in the AT&T ASIC library are all qualified for 3.3v. operation - making it a low risk approach to use in developing longer lifetime terminals.

AT&T has developed an evolutionary line of products for Digital Cellular markets. These are based on core DSP processing engines. Today's offerings include standard fixed-point DSPs, two new Signal Coding DSPs, and an integrated DSP + Codec single chip product. Also available is a Baseband Codec device which contains numerous A/D and D/A converters on one chip for performing control and baseband signal conversions.

Historically, AT&T has been an industry leading innovator in the area of single chip DSPs. Technological innovations led to the early design and introduction of the world's first integrated DSP + Codec. This chip, the DSP16C, was specifically designed for Digital Cellular applications. The voiceband sigma-delta codec converts speech to digital bit streams (and vice versa). The DSP can be used to perform speech coding as well as value-added functions such as echo cancellation, speaker recognition, speech recognition, and so on.

AT&T's Signal Coding DSPs, the DSP1610 and DSP1616, are further examples of application specific DSPs. These are 16-bit fixed-point DSPs with enhanced computation, bus and I/O capabilities. They have been designed specifically for performing the Channel Coding and Equalization functions in a Digital Cellular System.

The DSP1610 is a 'RAM-based' version (8Kwords, dual-ported), with no ROM on-chip. The DSP1616 is a 'ROM-based' version offering on-chip ROM (12Kwords) as well as some RAM (2Kwords). Both devices provide external access to both program and data space via a dual-ported memory configuration.

Designed into the Signal Coding DSPs are architectural features which enhance total system performance in a Digital Cellular application. These include:

- Sleep mode
- Dual-port RAM
- 2 Serial I/O ports
- Bit I/O unit
- Memory-mapped I/O
- Vectored interrupts with TRAP
- JTAG
- Bit Manipulation Unit
- Timer
- Source code compatibility with earlier DSP offerings

These features have been carefully selected and architected into the DSP with close cooperative definition by cellular customers. The objective is to achieve higher code density for better performance (e.g. lower power) and lower total system cost (less memory, etc.).

Note also that AT&T provides built-in hardware testing functions useful for system testing. JTAG test interfaces are included on all the new DSP products. There are hooks included on-chip for enabling full speed hardware emulation (up to 40 MHz).

In addition to devices, AT&T also offers complete software for the GSM 06.01 Speech Processing Functions (Speech Coding, Voice Activity Detection, Comfort Noise Insertion, Discontinuous Transmission). This software is available in source and has been tested and passes all GSM test vectors.

Extra processing bandwidth available in the DSPs can be used to perform value-added functions such as Echo Cancellation or Speech Recognition for handsfree operation. Software to perform these functions is also available.

The DSP16C, DSP1610 and DSP1616 are products designed using AT&T's proprietary Core Design Methodology. This is a design philosophy which enable DSP designers to customize

or create specific enhanced programmable DSPs with significantly reduced design and development times. This also illustrates the ability to provide timely evolutionary products. This methodology will be used in the development of future products - both standard and application or customer specific.

AT&T's process evolution (to 0.5µ drawn) will also add to future total system performance. By evolving to 0.5µ technology, low power (3.3v) devices will have the processing bandwidth to perfom all the computations required, and consume less power. For example, a 3.3v 0.5µ DSP will have the same throughput as a current 5v 0.9µ DSP and will consume about 1/3 the power (comparisons at 33 & 40 MHz).

AT&T also has migration plans for evolving the current multiple DSP solution into a future single chip solution. The objective is to achieve higher processing performance through higher integration and more intelligent architectures to enable lower total system cost and power consumption.

The T7582 Baseband Codec provides for A/D (Rx) and D/A (Tx) conversion of in-phase and quadrature baseband signals. There are additional D/A converters for control of the Rx/Tx functions. Also integrated on-chip in the receive path are Programmable Gain Amplifiers (software programmable form 0-18 dB in 2 dB steps). The device runs on a single 5v. supply and is available in a 44 PLCC package.

VII. Summary.

AT&T-Microelectronics has been closely following European Digital Cellular standards and market developments. AT&T is committed to supplying highly integrated, high performance products for system manufacturers. There are a number of products available today (design cells, devices, and software), and clear evolution paths for each product line.

AT&T's offerings are strongly based on customer inputs. Future products will also be based on customer inputs. The timing of product introductions has been and will continue to be timed for market stages.

Today, for the *Capability Demonstration* and *Product Differentiation Phases*, AT&T's offerings provide good trade-offs between integration, programmability and system performance (power, size, weight). Manufacturers can configure complete systems using AT&T technologies and can integrate a variety of value-added features for their end product differentiation.

In the future, manufacturers can look to AT&T for further integrated solutions with lower cost and superior system performance. New technology developments (e.g. 3.3v operation, 0.5µ CMOS, etc...) will enable AT&T to continue to offer leading edge, cost effective products.

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A 6.55 KBIT/S Multipulse LPC Speech Coding Scheme for Application in the Digital Mobile Radio System

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Summary

In this paper we present some results related to the design of a codec operating in the range 6.55 kbit/s to 7.55 kbit/s. This codec configuration may be suitable for application in mobile telephony systems, since for this application high quality speech (8 Khz sampling frequency) at bit rates below 16 Kbit/s is a prerequisite. For example, the GSM pan-european digital mobile radio system has been defined with the capability to use alternatively both full rate and half rate channels, and the net bit rate expected for the half rate source coder is around 6.5 Kbit/s. At this bit rate one of the most suited speech coding technique seems to be the Multipulse Linear Predictive Coding(MP-LPC). However, several different schemes can be implemented. depending on the actual bit rate, the considered sub-frame length, the parameter update rate, the techniques adopted for both the LPC parameters and the excitation sequence, and so on. Various simulations were carried out, taking into account evaluation criteria like subjective quality of the synthesized speech and feasibility of the real time implementation. The adopted final scheme consists of:

*) An LPC identification step using the autocorrelation method, thus allowing the parameter quantization to be performed in a single step using a properly designed vector quantizer.
*) The long term prediction (LTP) block computation using an open loop configuration, in order not to be constrained by the frame length.
*) The excitation computation using an optimal procedure recently developed by Singhal and Atal.
*) The excitation sequence quantization by means of a scalar quantizer derived from the pulse amplitude distribution.
*) A post-filter in order to cope with the high frequency distortions of the synthetic speech.

Coder description

A block diagram of an LPC based speech synthesizer with multipulse excitation, is shown in fig.1. The excitation signal u(n) is fed into a cascade of two synthesis filters which carry the long term and the short term information respectively, to produce the output synthetic speech s1(n). The resulting error signal between s1(n) and the original speech s(n) is suitably weighted and fed back to the excitation generator. The excitation generator computes the pulse amplitudes and locations such that the weighted error between original and synthetic speech is minimized. This closed loop procedure is referred to as "analysis-by-synthesis technique". The information to be transmitted to the receiver consists of the filter coefficients and the excitation amplitudes and positions.

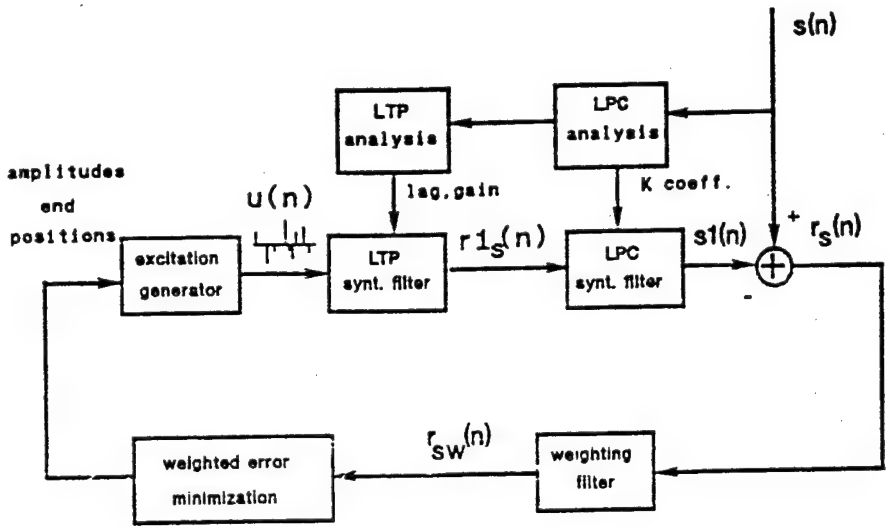

Fig.1. MP-LTP-LPC coder

LPC analysis block

LPC analysis consists of the vocal tract model identification,by means of suitable parameters,which are the coefficients of an all pole filter given by [5][6]:

$$\frac{1}{A(z)} = \frac{1}{\sum_{k=0}^{p} a_k z^{-k}} \qquad a_0=1 \quad , \quad p=filter\ \ order$$

this has been the most widely used model to characterize the spectral envelope of the vocal tract. With such a model the nth speech sample prediction s1(n) is considered to be a linear combination of past samples:

$$s1(n) = -\sum_{k=1}^{p} a_k s_{n-k}$$

The error between the actual value s(n) and the predicted value s1(n) is given by :

$$r_s(n) = s(n) - s1(n) = s(n) + \sum_{k=1}^{p} a_k s_{n-k}$$

and is known as the "short term residual". When the filter 1/A(z) is driven with the residual, it produces exactly the original speech signal s(n). At bit rates lower than 8Kbit/s the number of bits available for encoding the residual is less than 1bit/sample, and the key issue in designing coders is finding efficient ways of representing the residual.

LPC parameters identification and vector quantization

In multipulse algorithms, more than half of the total bit rate of 6.55 Kbit/s is reserved for the residual excitation information. This doesn't leave much for the linear predictive filters coefficients. With a properly designed vector quantizer, coding of the LPC prediction parameters can be made accurate enough. In vector quantization the quantizer looks up in its memory the set of coefficients which best matches the LPC predictor, according to a proper distortion measure. Then it chooses the address code stored in the memory's codebook for the matching set parameters. In our model the analysis frame length is 160 samples long (20 ms), the LPC filter order is 10, and the codebook contains 1024 candidate set of parameters (corresponding to 1024 vocal tract models). The the quantizer needs only 10 bits to transmit a sequence of 10 quantized coefficients, and the quantization rate is only one bit per parameter. The codebook was generated by using the LBG algorithm [4], an iterative process that minimizes distortion over a large number of test frames of speech. In the training process a vector representing the LPC parameters was calculated for each frame, then the 1024 most rapresentative vectors (centroids) were chosen to be quantizer elements. In building the codebook the "Itakura-Saito" distortion measure was used [1][4][5].

Long term prediction block

The multipulse model treats all types of speech sounds with the same excitation structure. This generality gives great flexibility to the multipulse algorithm, which can adjust the pulses in a way to generate the periodicity of the voiced speech.In spite of this capability, the use of a long delay predictor between the LPC all pole filter and the excitation generator is useful for two reasons:

1) experience shows that about 8 pulses are needed per pitch period in multipulse excitation for high quality standards. This implies that female speech requires more pulses per frame than male speech,for comparable quality.

2) at low bit rates, only a few pulses are available, and multipulse algorithm uses all of them to recovery the periodicity of voiced sounds. instead of adjusting them to compensate for the LPC predictor inaccuracy .

The two analysis predictors configuration uses a cascade of the formant predictor and a pitch predictor, as shown below.

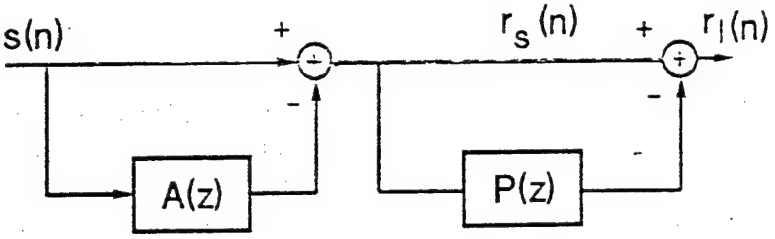

Fig.2. LTP-LPC analysis cascade

This structure, with the short term analysis first, can be explained with a standard speech production model; in fact, the pitch periodicity is still present in the residual signal, while if the long term redundancy was subtract first, the speech spectrum would be influenced, affecting the formant accuracy.

The pitch predictor expression is:

$$P(z)=\beta z^{-M}$$

where ß and M are the predictor gain and lag respectively. The long term residual is obtained by subtracting the scaled (factor ß) and delayed short term residual from itself.

Pitch, lag and ß estimation

It can be noted that the scheme shown in fig.1 uses, for ß and lag estimation, an "open loop" configuration. In fact the LTP filter parameters are determined during the analysis step, and they do not partecipate in the weighted error minimization loop. The model below demonstrates how the predictor coefficients are calculated:

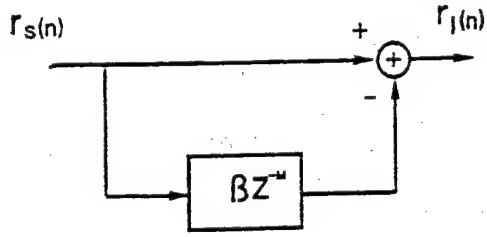

Fig.3: lag and ß calculation model

The squared mean error is defined as

$$\epsilon^2 = \sum_{n=-\infty}^{+\infty} r_l\,(n)$$

and if we refer to the lattice formulation of the predictor , it can be espressed as :

$$\epsilon^2=(1-\beta^2)$$

where ß is given by:

$$\beta=\frac{2\Phi(0,M)}{\Phi(0,0)+\Phi(M,M)}$$

and

$$\Phi(i,j)=\sum_{n=0}^{N-1} r_s(n-i\,)r_s(r-j\,)$$

N being the analysis frame length. Then, ϵ^2 minimization leads to a lag choice, M, such that β^2 is maximum. With this formulation the reflection coefficient ß always has magnitude smaller than unity and the resulting filter is stable.

This open loop configuration has been compared with the closed loop one described by Atal in [8]. In this case the pitch predictor is determined in an "analysis-by-synthesis" way and the predictor parameters are chosen to contribute to the weighted error minimization. The optimum pitch delay is obtained by setting the multipulse excitation to zero, and filtering

the signal r1(n) with the LPC predictor for each possible lag value. The value minimizing the weighted error is chosen. During this procedure the gain factor is set to one.
Error minimization with respect to ß leads to an expression which is used to find the optimum gain once optimum lag is known. This procedure may give a |ß| value greater than one, producing an instability.

Comparison of the results
Comparison of the two configurations, open and closed loop, was tested under these conditions :

*) analysis frame length: 160 samples (20 ms)
*) lag was varied in the range from 2.5 ms to 18.375 ms, corresponding to 20 and 147 samples, for the open loop case
*) lag was varied in the range from 20 ms to 35.875 ms (160 and 287 samples) for the closed loop case.
*) 3 bit uniform ß quantization plus 1 sign bit
*) simulations were carried out with a data base including two minutes of female and male voices

results are the following:

*) the closed loop configuration shows a segmental SNR improvement of about 0.5 ≈ 1 dB
*) subjective quality is drastically worse in the closed loop case, especially for female voices. This is probably due to the fact that in the closed loop scheme the minimum lag is lower bounded to the frame length. Therefore if the pitch frequency is high, the long term predictor only recovers a periodicity that is multiple of the actual one. This problem could be solved by shortening the analysis frame, but this would require a more frequent updating of the predictor parameters and an increased bit rate.

For these reasons the open loop configuration shown in fig.1 was the final choice.

The multipulse block
Multipulse excitation represents the residual as a sequence of a few pulses per frame, located at non uniformly spaced intervals. The pulses are not specified a-priori but are computed on a frame by frame basis by minimizing the energy in the weigthed error signal. The number of pulses placed in each frame depends on the desired speech quality. The more pulses per frame, the better the output quality. In our simulations we found that, by employing the pitch predictor described above, 17 pulses per frame produced a quality as good as the one achieved with the GSM full rate algorithm, and the required bit rate is 7.55 Kbit/s. In order to reduce the bit rate to 6.55 Kbit/s, only 13 samples per frame have to "survive".

Excitation computation
The excitation analysis procedure has to determine both amplitude and position of the pulses. The pulses amplitude can be easily obtained with equations similar to those used to compute the all pole predictors [5]. However, computation of pulse locations is a combinatorial problem with no closed form solution. If the number of pulses per frame is m, and the frame

length is N, an exhaustive search for the pulse locations is impractical, since it requires the solution of

$$\frac{N!}{m!(N-m)!}$$

linear systems of the mth order. Among the sub-optimal algorithms proposed in literature, we selected the "optimal amplitude method", recently developed by Atal and Singhal in [8].

The weighting filter W(z)

It becomes increasingly difficult at low bit rates to accurately match the speech waveform. Consequently, the mean squared error between the original and the reconstructed signal is less meaningful. Frequency masking experiments demonstrated that the human hearing system has only a limited capability to detect small errors in the frequency bands where the speech signal has high energy, as in the case of formant regions. Hence, to make use of the masking effect, the noise has to be distributed in relation to the speech power over the different frequency bands. The commonly used weighting function is given by:

$$W(z)=\frac{[1-\sum_{k=1}^{p} a_k z^{-k}]}{[1-\sum_{k=1}^{p} a_k \delta^k z^{-k}]} \qquad 0\le\delta\le 1$$

where the δ parameter controls the error increasing in the interformant regions. The use of the proposed filter makes possible a simplified structure for the analysis-by-synthesis loop, as shown in fig.4.

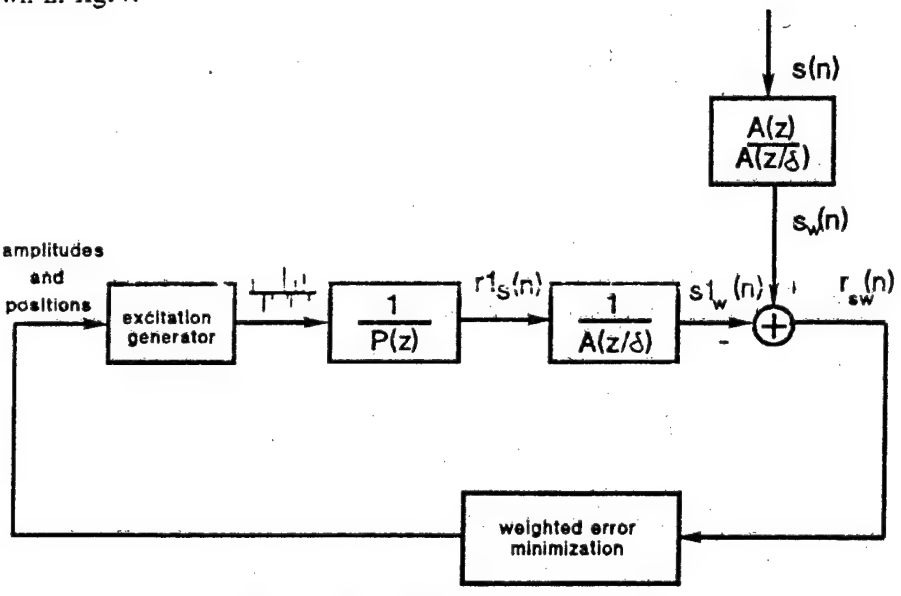

Fig.4. Simplified coder scheme

The decoder

Because of the coder structure, the decoder is very similar to the decoding part of the analysis-by-synthesis loop. In fact it consists of the cascade of the LTP and LPC filters driven by the quantized multipulse excitation sequence.

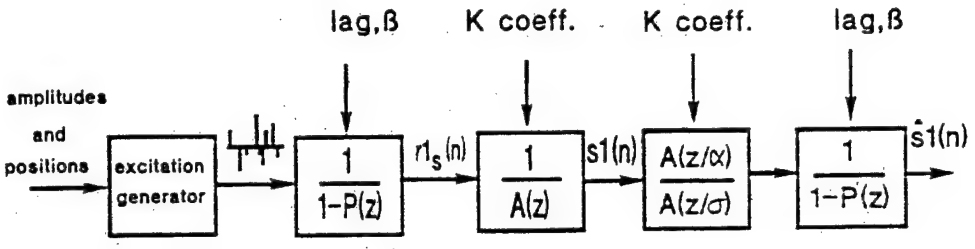

Fig.5. Decoder

Fig.5 shows two further blocks corresponding to a postprocessing of the reconstructed voice s1(n). The coder discussed above can operate at a variable bit rate, depending on the number of non zero pulses in the multipulse excitation. Below 8Kbit/s (correponding in our model to about 18 pulses per 20 ms frame), the quality starts to degrade, with a degradation that is perceived as that of a signal corrupted by additive noise. One way to reduce this effect is to emphasize spectral peaks, both in the envelope and in the fine structure. This is the function of the two postfilters which "reinforce" the LPC and LTP spectrum peaks. The postfilters expressions are [3]:

$$\frac{A\left(\frac{z}{\alpha}\right)}{A\left(\frac{z}{\sigma}\right)} = \frac{[1-\sum_{k=1}^{p}\alpha^k a_k z^{-k}]}{[1-\sum_{k=1}^{p}\sigma^k a_k z^{-k}]}$$

and

$$\frac{1}{1-P'(z)} = \frac{1}{1-\tau\beta z^{-M}} \qquad 0\le\tau\le 1$$

Listening tests led to the following choices:

$$\alpha = 0.5 \qquad \sigma = 0.8 \qquad \tau = 0.3$$

Quantization and coding

It can be noted from fig.5 that, for synthetic speech reconstruction, the decoder needs the LPC and LTP parameters and the multipulse excitation. As described earlier, the LPC model consists of 10 reflection coefficients, vectorially quantized by means of 10 bits. Concerning the LTP parameter, we used 7 bits for the lag information, which allow a lag excursion from 20 to 147 samples, corresponding to a pitch frequency of 400 and 54 Hz, respectively. The ß gain is linearly quantized with 4 bits plus 1 sign bit. Updating of the synthesis filters coefficients is performed every 20ms (once per 160 sample frame), leading to a bit rate of 1100 bit/s for the prediction part. Thus there are approximately 5400 bit/s left to describe the multipulse excitation. The following quantization was used :

*) 13 pulses are transmitted every 20ms

*) the maximum value among the pulses is computed and logaritmically quantized with 6 bits plus one sign bit; its position among the 13 pulses is quantized with 4 bits.

*) the other 12 pulses are normalized to the quantized maximum value and optimally quantized with 3 bits. For this purpose we used a statistic obtained with a training set containing 6 male voice files and 6 female voice files, of 1200 frames each (24 s). The resulting statistic, shown in fig.6, was generated using the output of the Atal algorithm when the pulse number is set to 13. The quantizer levels were obtained by partitioning the total area into four equal sub-areas and finding their centroids. One more bit per sample is needed for the negative part of the quantization characteristic.

*) Coding of all possible configurations of 13 position among 160 requires

$$\log 2 \binom{160}{13} = 62 \quad bit$$

The multipulse excitation therefore requires 62 + 12 x 3 + 1 + 6 + 4 = 109 bits every frame, hence 5450 bit/s which, added to the 1100 bit/s required for the prediction section give a total bit rate of 6.55Kbit/s.

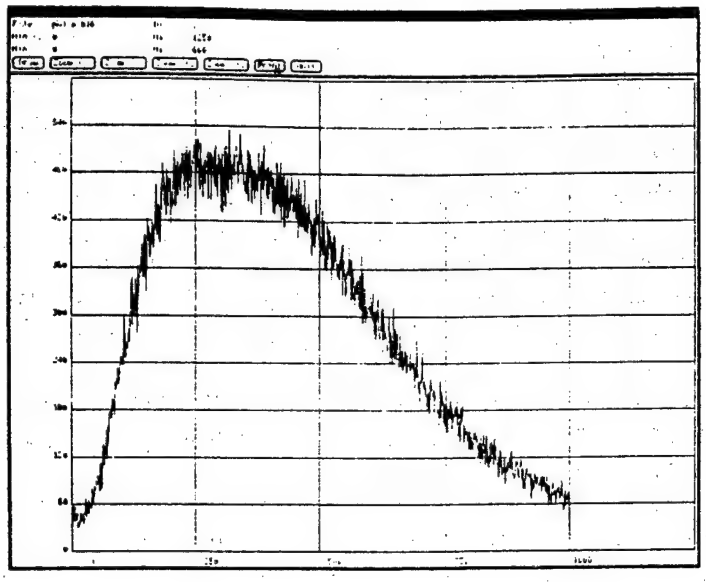

Fig.6. 13 pulse amplitudes statistic

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ARCHITECTURE AND TECHNOLOGY APPLIED TO FLEXIBLE BSC

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Abstract

This paper describes the Base Station Controller (BSC) system developed according to GSM recommendation by Siemens Telecomunicazioni S.p.A.; both for hardware and software, the technological characteristics and the innovating system concepts, that distinguish it, are pointed out.

1. Introduction

The architecture of the BSC described in the following has been designed in a flexible way in order to meet the characteristics of various kinds of station and network admitted by the present standards.
The choice to decentralize as far as possible the processing functions into peripheral units allows a good load sharing among the processors used and therefore the total throughput can be tailored on the number of radio terminals.
In this way a modular BSC is born with the capability of handling 64 up to 1000 traffic channels and possibility to drive either colocated or remoted Base Transceiver Stations (BTS).
The article is expressed in two parts: the first one is relevant to the hardware characteristics, while the second one deals with the software analysis.

2. Hardware Architecture

This base station controller has been developed around a basic block which implements the centralized control functions; in order to guarantee high system reliability this block is fully duplicated. The peripheral functions and the interfaces with to the Base Transceiver Stations and to the Mobile Switching Center (MSC) have been implemented by modular design to achieve a proportional growth between performance and cost-power consumption.
A functional block diagram of the BSC is shown in the figure 1; the above mentioned basic block comprises:

- the Main Processor with the relevant Mass Storage and the Operating and Maintenance Interface,
- the Telephony Processor,
- the Switching Network,
- the Clock unit.

The peripheral functions are implemented by the LAPD Processors and by the Common Channel Signalling System N. 7 Processors; the interfaces with BTS and MSC are realized by PCM Interface units.

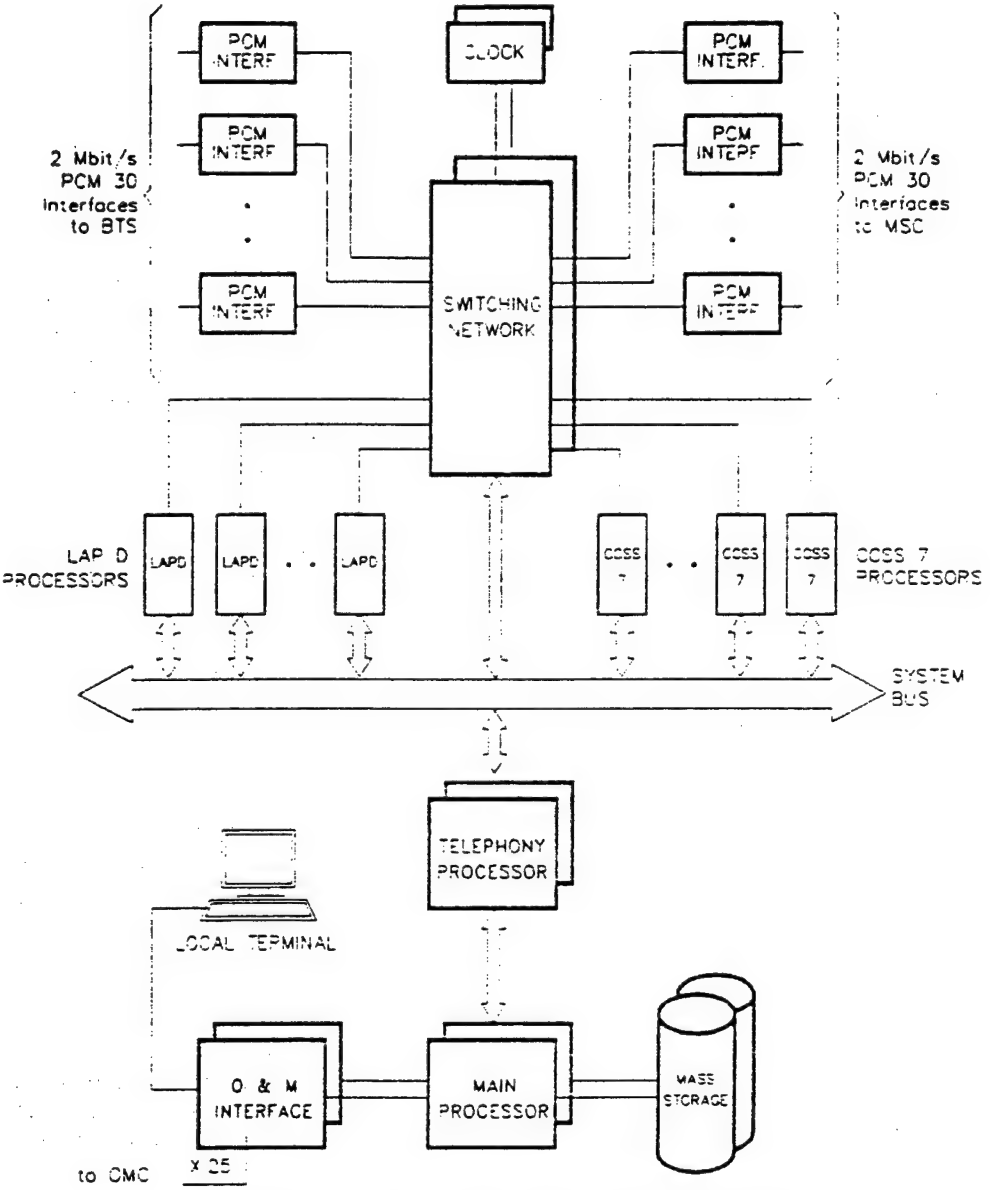


Fig. 1 - BSC FUNCTIONAL BLOCK DIAGRAM

In the following each block of the diagram will be briefly described.

The Main Processor acts as the administrative processor of the BSC, that is it supervises the right operation of the system by means of proper routining and audit, manages the reconfiguration in case of fault and dialogues with O&M center for configuration control, traffic and quality of service reporting, faults monitoring and so on.

The Main Processor is implemented by three cards: the microprocessor circuit, the external memory and the bus extender.

The microprocessor circuit is realized by a 16 bit microprocessor with 1 Mbyte of dedicated memory on board and a "configuration control logic" that resolves via hardware which copy of the processors must be

active; in order to increase the reliability a fast fault-detection circuitry is also implemented.

The external memory has a capability of 2 Mbytes; both copies of memory can be updated contemporaneously by the active processor, allowing the availability of a hot stand by copy of data at any time. The bus extender provides the suitable driving capability of the microprocessor bus to the external units, like peripheral processors, PCM interfaces, switching network and clock generator.

The Mass Storage unit is realized in a single board and it can be seen as logically belonging to the main processor area; at the present it is implemented by a 40 Mbyte hard disk. A HDLC (High Level Data Link Control) channel interconnects the two disk copies in order to allow the updating of the stand by copy under the control of the processor inside the active one.
The disk will contain the programs of all the down-loadable processors (including the BTS processors), the data base of the BS (Base Station) system, the maintenance reports, the operating and statistical data.

The O&M Interface also belongs to the main processor area and it is implemented by one card; this unit connects the administrative processor to a remote O&M center by a CCITT Rec. X.25 interface and to a local terminal by a RS232 link. An on board processor implements the level 1 and level 2 functions of the X.25 data link and manages the communication protocol with the local terminal.

The highest throughput is provided by the Telephony Processor; the principal functions of this processor are call handling, signalling management (level 3 MTP), radio resources management and handover management; besides these telephony functions it realizes a message distribution function towards the peripheral processors (LAP D, CCSS7). Two cards have been used for this processor; one for the telephony processor and message distributor with a 1 Mbyte built in RAM and the other one for an external 2 Mbyte RAM; each copy of the telephony processor is internally duplicated for a fast fault detection, moreover the external RAM can operate in active/hot stand by configuration.

The Switching Network implements in a single board a square matrix for 3072 digital signals at 64 Kb/sec; it provides a space-time-space matrix by means of a single stage matrix operating at 24 MHz.

The Clock unit provides all the units of the system with clock and synchronism signals; it can operate either in asynchronous or externally synchronized mode; the oscillator circuit is a DPLL (Digital Phase Locked Loop) and the accuracy of the frequency delivered is better than 5x10 exp(-9) (hold over mode).

The CCSS7 Processor is responsible for handling the MTP (Message Transfer Part) layer 1 and 2 of the Common Channel Signalling System N. 7 protocol used for signalling on the A interface; up to four data links are processed per card.

The LAP D Processor handles the layer 2 of the LAP D protocol used for

signalling on the A-bis interface; moreover some layer 3 functions of the BTS management (measurement result handling) are implemented; up to four LAP D signalling channels are implemented in a card.

The PCM Interface realizes the interface between the BSC switching network and the BTS and/or the MSC according to CCITT Rec. G.703, with traffic channels and data links at 64 Kb/sec; up to eight interfaces are implemented in a single board.

Notice that for reliability the peripheral processors (CCSS7, LAP D) and the PCM interfaces operate with N+1 redundancy with automatic reconfiguration in case of fault.

3. Circuit Design Guideline

Developing the BSC, some basic objectives have been pursued in the system and circuits design:

I) high reliability
II) high performance
III) reduced size
IV) low power consumption
V) modularity

Reliability has been improved by full duplication of centralized functions and by N+1 redundancy concept for the peripheral functions, as above mentioned; furthermore all interconnection busses are duplicated and each copy is parity protected. For fast fault detection alarm circuitries are contained in each card of the system, in particular regarding the administrative and telephony microprocessor's monitoring, it must be noted that two microprocessors (per copy) operate synchronously and a comparison circuit indicates the faulted copy as soon as a mismatch between basic signals is detected.

Two ways have been followed in order to implement a high performance system: the first one consists of equipping the processing critical area (i.e. telephony processes) with a powerful processor, the second one is to share as far as possible the processing load among several processors (i.e. peripheral processors like LAP D and CCSS7); this last approach supports the objective of the modularity.

The interprocessors communications have been implemented by means of "dual port RAM" in order to minimize the waiting time for processor's synchronization and messages exchange.

Furthermore dedicated VLSI IC's are used to realize by hardware the lowermost signalling protocols (i.e. LAP D and CCSS7) thus avoiding real time consumption of the relevant processors; following the same guideline a special processor has been designed, based on a DSP (Digital Signal Processor), to handle the measurement results.

To reduce the system size and the number of cards, the packaging of circuits per cards has been increased by means of a large use of surface mounting devices, of VLSI logics when available, of programmable logics (i.e. for chip selects and 32 MHz bus tracker of the telephony processor) and gate arrays as far as possible.

Six types of ASIC have been developed of 1.5 µm technology and up to 12.000 gates; by means of these gate arrays it was possible to implement large and very complex circuits is a single board (as eight PCM interfaces, a 3072 channels switching matrix, the telephony processor and four LAP D/CCSS7 processor).

The power consumption has been contained using as far as possible standard IC's of the families HC, AC, HCT, FCT and ASICs.

As above said a suitable modularity has been reached by centering in a base module only the capital functions and, in particular, by implementing in a single processor only the indivisible processes, while the peripheral functions has been distributed among several units of few different types.

4. PC Board and Backplane Technologies

Most cards implementing the BSC are 6-layer Printed Circuit Boards (PCB), manufactured using FR4 as a dielectric. The main characteristic of the layout is the conductor width of 8 mils with a minimum clearance of 8 mils.
Almost all components are Surface Mounted Devices (SMD). Both sides of the PCB are used for components; thus it was possible to obtain high density cards (fig. 2). As an example, the Octal Trunk PCM Interface card houses 512 components, 1960 connections and 1598 holes in a 208x330 mm PCB, which gives a density of 4.84 components per square inch (fig. 3).

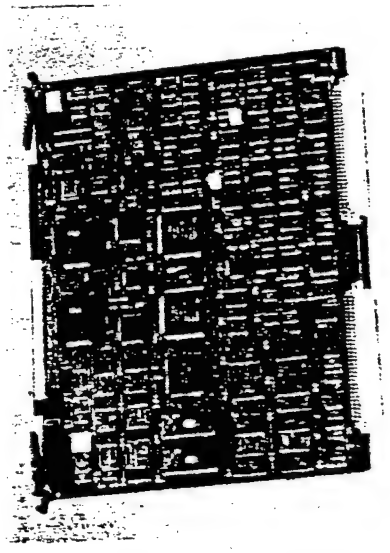


Fig. 2: Telephony Processor Card

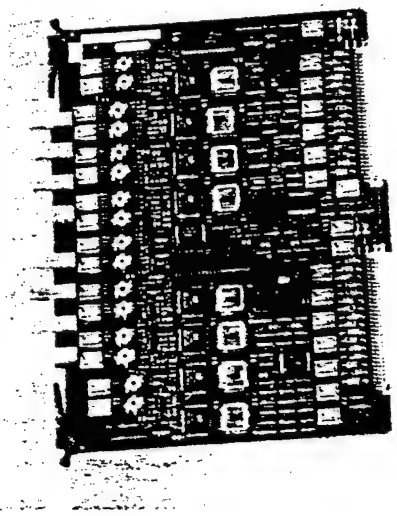


Fig. 3: Octal Trunk PCM Interface Card

All cards are designed for automatic mounting and all electrical nodes are accessible from the solder side to facilitate the in-circuit test. The Power Supply is equipped in an aluminum casting. This permits to dissipate the heat and to shield the electromagnetic emission. Moreover to reduce EMI from the different types of circuit, a particular care has been taken to properly ground them and to avoid electric loops.

The backplanes, that provide all the internal connections, also leads signals to the input/output connectors. The backplane is a fourteen-layer pcb with four layers for power and ground and ten layers for signals and is manufactured using FR4 as a dielectric.
The backplane is 430x700 mm (wxh) with 8 mils line space, holes of 0.6 mm and pads of 1.02 mm.This means that the maximum tolerance, i.e. sum of all manufacturing processes must be within +/- 0.1 mm over a length of 800 mm.

In the backplane of the base module there are 3276 connections, 9997 holes and 86 connectors (Siedecon 256 pins for cards, DIN type for power supply, coaxial for PCM lines, sub D connectors for standard interfaces).
The interconnections with the expansion modules are made by means of high density connectors (16 connectors with 100 pins each) and flatcables.
The flatcable wires are used alternately for signal and ground to reduce crosstalk.

To avoid crosstalk between switching and quiet lines, and long bus-settling times because of stub ringing and capacitive loading and to reduce signal reflections, the backplane interconnections have been disigned as transmission lines.
The transmission line has well defined electrical properties per unit length, which are constant over a wide range of frequencies.
The transmission lines used in the backplane are microstrip on the external layers and asymmetrical stripline in the internal layers. The characteristic impedance is 65 ohm.

The signals in the backplane have been divided according to their particular functions and sensitivity. The main signals families are: processor busses, clock, commands (strobe, clear, write, etc.), PCM lines, continuous signals.

5. Frame Structure

The mechanical dimensions of the rack are in accordance with the ETSI standard (h=2200, w=600, d=300 mm).
The rack enables the cabling to be routed either over a cable support structure or under raised floor.
The fixing subracks mounting width is 515 mm and the mounting pitch is 25mm.

Subrack dimensions are h=700, d=250, w=535 mm (432 mm internal). It is compliant with EMC std EN-55022-B. To obtain this, all

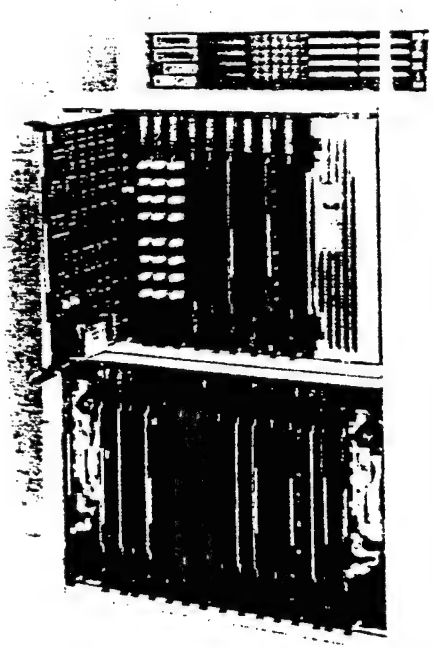


Fig. 4: Base Module Fully Equiped Without Front Panel

the apertures are sealed with contact springs and soft shielding gasket.
The maximum allowable heat dissipation in a subrack with natural convection is: 300 W with a ΔT of 25° K (fig. 4 - 5).

6. Software Architecture

The BSC software architecture is based on the distributed processing scheme of the system. The allocation of functions to the different processors is related to the layered structure of the protocols used in the GSM system.

1. The peripheral processors PPLD and PPCC implement the level 2 of the protocol stacks toward the BTS (Lapd) and the MSC (CCITT SS7) respectively.

2. The TDPC processor implements the level 3 of the SS7 protocol toward the MSC and the procedures specified by the Mobile Application Part (MAP).

3. The LXLT processor implements the lower level of the OSI stack toward the Operation and Maintenance Centre (OMC). It also implements the interface to the Local Terminal PC.

4. The MPCC processor is mainly devoted to the Operation and Maintenance procedures, as directed by the OMC. It also performs the local supervision of the system, in terms of hardware status handling, fault detection and recovery, in order to ensure the required fault tolerance and reliability of the system.

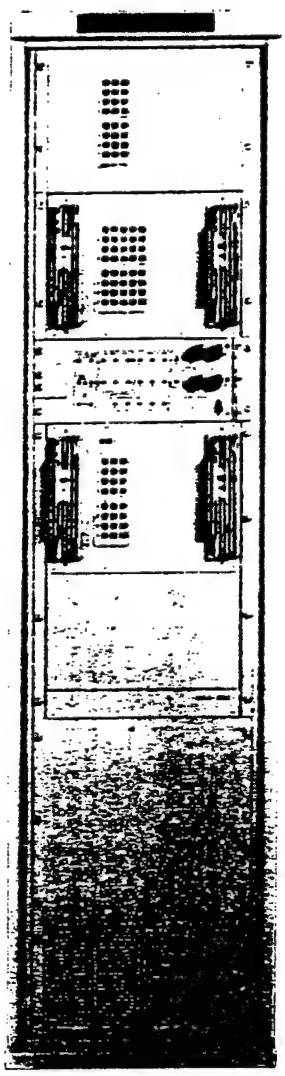


Fig. 5: BSC Rack Fully Equiped with Base and Expansion Module

Because of the specific hardware structure, the MPCC also controls the physical setting of digital connections through the switching network for either voice, user data and signalling. It is to be noted that, because of processor load balancing reasons, some of the MAP functions, to be performed on a radio link basis, are allocated in the peripheral PPLD processors. In particular these functions are related to the handling of quality measurements and to the algorithm to initiate the handover procedure.

The system functions are carried out with the contribution of all or some of the processors. An interprocessor message communication mechanism is implemented so that processes running in a given processor can activate processes in other processors.

The software organization in each processor reflects its functional role in the system architecture. Considering the central processing units (MPCC and TDPC), the following software decomposition has been implemented :

1. The design of the Operating System software is common to the two processors, the source code is unique and is compiled for the different CPU's (using conditional compilation where needed).

2. The MPCC software, which mainly performs administrative and maintenance functions, is decomposed into the following packages:

   a) STATUS MANAGER to keep under control the Operational status of all hardware devices in the system, processing either internally or externally initiated status transition requests. Alarm reporting functions are also implemented in this package.

   b) SYSTEM MAINTENANCE, providing hardware recovery functions (fault detection, fault isolation and service restoration) and hardware diagnostic procedures. It should be noted that the MPCC is the master processor in driving all the recovery and diagnostic processes for all system hardware.

   c) DATA BASE ADMINISTRATION, providing procedures for initializing the system configuration data and the operational parameters driving the system features.

   d) NETWORK CONTROLLER, to set-up digital connection between the A and the A/bis interfaces, as directed by the call processing software in the TDPC processor.

   e) ADMINISTRATIVE SOFTWARE, whose main function is to provide statistical reports of the system behaviour.

3. The TDPC software, which mainly implements the MAP procedures (call control, radio resource handling, etc.), is decomposed in the following packages:

   a) SS7 SIGNALLING, providing the Level 3 layer (Message Transfer Part and Signalling Connection Control Part) of the protocol used to interface

the MSC on the A interface.

b) LEVEL 3 RADIO, implementing the procedures of the Mobile Application Part for what concerns the BSC, as specified by the GSM recommendations.

c) Each software package resident in the MPCC, except for NETWORK CONTROLLER, have a counterpart in the TDPC which acts as "slave" of the MPCC resident "master". For example, a Data Base update process is driven by the DATA BASE ADMINISTRATION software in the MPCC, which may activate a "slave" process in the TDPC to update the TDPC resident portion of the Data Base affected by the change.

7. Operating System

The BSC system software runs under control of a proprietary Real Time Operating System Kernel called RTE+ (Real Time Executive). This allows the implementation of a real time, multitasking,interrupt and/or polling driven system, optimized for the INTEL family of CPU's (8086/80186/80386).

RTE+, as any real time kernel, is basically a resource manager, the managed resources being :

1. CPU time (real time)
2. System Memory (dynamic allocation of memory areas)
3. Task communication and synchronization devices (mailbox,semaphore, event)
4. System Timings

RTE+ directly handles these resources, and provides the application programs with the system services for their use. RTE+ is mainly implemented in "C" language, some critical routines being written in assembly language. Specific hardware dependent routines are coded using conditional macro expansion, in order to implement different code depending on the particular target. The application programs are seen be RTE+ as TASKS to be scheduled according to a given policy. Periodic Tasks are executed on a cyclic basis at a high priority level, Prime Time Tasks are executed on the occurrence of real time critical events, Spare Time Tasks carry out non real time critical activities and are executed when CPU time is available.

RTE+ includes configurable components, which are allocated and initialized at System generation time. These components are basically tables describing to RTE+ the tasks it will have to run, including their attributes (task types, priority schemes,task entry points, scheduling parameters, etc.).

Many application programs are specified and implemented using SDL (the CCITT Specification and Description Language). RTE+ supports the virtualization of a Finite State Machine by means of a particular Prime Time Task (the FSM task) inside which all of the SDL processes are executed.

The translation from the SDL specification to the "C" language code is then made extremely straightforward: a one to one relationship exists between a given SDL process and the "C" module implementing the state transitions defined in the SDL process itself.

The FSM Task basically distributes the incoming events to the procedures that execute the actions to be performed for the combination of the received event and of the current state of the destination process.

RTE+ also provides I/O drivers in order to decouple the design of the FSM task from the specific hardware periphery from/to which external events are gathered/forwarded.

8. Software Development Methodology

The selected software development methodology takes advantage of the available CASE technology in order to improve designer productivity and to facilitate an orderly growth of the software product both during the initial development and through design maintenance phase (including incremental addition of new features).

To improve the software specification phase of the design, a commercially available SDL based CASE tool has been used. Its interactive graphic editor allows the designer to specify the SDL system in terms of its structure ("blocks", "processes", their hierarchy and interconnections), and of the behaviour of the defined processes.

The tool interactively verifies the SDL syntax and the static semantic of the system description. It is also possible to verify the dynamic behaviour of the system by means of simulation running on the host machine.

The tool also provides automatic generation of "C" code; this feature has not been used because of the peculiarity of the target execution environment. Also the high optimization required by a real time application suggested a non automated coding phase.

Using the one to one relationship between SDL processes and "C" modules, a testing tool has been developed which can interact with the SDL processes running on the target machine. The tool can simulate sequences of messages, on the A and A/bis interfaces according to the GSM procedures, and verify the correctness of the behavour by analyzing the messages received back from the system.

9. Software Configuration Management

The software development environment has been set up giving particular emphasis to the software configuration control aspects. Again a commercially available CASE tool has been selected which was considered able to provide the Configuration Management procedures required to support the life cycle of a rather large software project.

This tool is built around a relational data base system which is used as a repository for all of the software components. These components are described in the data base according to the functional breakdown of the system. Design parts of a specified type are associated to each level of the decomposition, and a predefined number of physical files (typically containing documentation and/or code) are associated to each design part type. In this way all hierarchical and usage relationships between components are stored in the data base.

The evolution of all components takes place according to predefined rules (each type of component has its own lifecycle); components may have many issues separately controlled by the Configuration Management system.

The generation of the software system is assisted by automatic build procedures using a baseline mechanism to appropriately select the components according to a predefined criterium. This is normally based on the lifecycle status of the components to be selected.

Changes needed to correct faults and to implement new features in one or more configurations of the system are handled by a change control system by means of "change documents". These basically describe problems found or requests of enhancements and the solutions introduced in the software. The change control system keeps track of the changes by relating each change document to the affected design part and to the components which are modified or created.

10. Conclusion

Innovative system design applied to hot duplication and fast fault detection together with a high density of packaging (both for large use of SMD components and ASIC and for PCB designed to the limits of manufacturing technology) have permitted to obtain a very suitable BSC, both for reliability and reduced size, that is able to handle from 64 to 1000 traffic channels with gradual growth.

The organization of the software easily allows the mapping of system features into software modules.
This in addition to the SDL approach to design and implementation greatly simplifies the addition of new features. The configuration management procedures also allow the generation of variants and multiple version of the system.

OSCILLATORS FOR GSM GROUND BASE STATION

JP AUBRY, G WAGNER and V CANDELIER
CEPE Compagnie d'Electronique et Piézoélectricité
44 Avenue de la GLACIERE 95100 ARGENTEUIL

The GSM program requires specific oscillators to be installed in the ground stations.

Due to various GSM ground base station design, the target specification requires either ovenised or temperature compensated oscillators

CEPE has a hughe experience in design and production of clock, temperature compensated and ovenised oscillators, for commercial and military markets.

Technologies available in CEPE, such as doubly rotated quartz crystal cut, surface mount printed circuit boards, monolithic thermal structure, PID thermal loop..., have to be used to meet the GSM specifications.

We present in this paper, as an exemple, the design procedure and the electrical performances obtained with small ovenised oscillators, for which sizes has been reduced to 40*30*19 mm^3 (type 1) and to 40*30*16 mm^3 (type 2).

Results of qualification of these oscillators will also be described.

GENERAL REQUIREMENTS

The main characteristics to be achieved are :

- small size
- fast warm up
- high temperature stability
- low ageing
- low cost

These requirements can be founded difficult to achieve in the case of ovenised oscillators.

Our current production of professionnal ovenised oscillators is mainly based on two families, PMT P and PMT.

The latter one, PMT, exhibits a size of 51*41*25 mm^3. In order to propose smaller sizes, CEPE has developped two new oscillators.

The sizes has been reduced to 40*30*19 mm^3 (type 1) and to 40*30*16 mm^3 (type 2).

The technology for the oven construction is based on the thermal regulation of a metallic volume acting as a common enclosure for the resonator and the first stage of the oscillator.

The resonators are SC cut 3rd overtone in the range of 10 to 20 MHz in HC 37 can for the PMT and type 1 oscillators, and SC cut fundamental in HC 18 for the type 2.

DESIGN PROCEDURE

Figure 1 gives the general structure of an ovenised oscillator. There are 6 main parts to be considered :

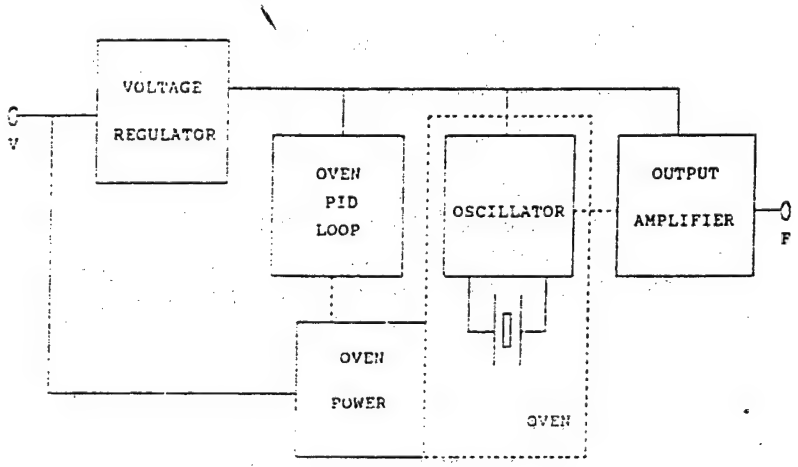


Figure 1

* the oscillator itself, including the crystal resonator, which is the real "signal generator",

* the output power stage acting as an isolator stage between the oscillator and the load, and giving the final shape to the signal,

* the oven control network whose role is to drive the power heating elements,

* the power elements, which are dissipating heat power to the metallic oven,

* the oven,

* the voltage regulator.

All of these elements are to be consired individually to be optimized and the overall stucture have also to be worked on because of the "inter-element" mutual reaction of their performances regarding the GSM oscillator specifications.

The following table gives the sensibility criteria between the oscillator structure and the key points of the GSM oscillator specification

		Xtal	Osc	OA	OL	OV	VR
F vs Temperature	***	**		**	**	***	
F vs load			**	***			
F vs supply voltage			**	*	**		***
F vs time (ageing)		***	***		*		**
warm up		***	*		***	***	
power consumption	**				***	*	
phase noise	**	***	**	***	**	***	
size		***		*		**	*

where OA stands for Output Amplifier, OL for oven loop, OV for oven, VR for voltage regulator.

The number of stars is an indication of the degree of criticity of the sub-fonction (colomn) versus the sub-electrical specification (line).

One san see in this table the inter dependance of the various design parameters for the overall specification.

From this table, the choise of the crystal resonator acts on the frequency (F) vs temperature (T) behavior, on the warm up characteristics, on the ageing, on the phase noise and indirectly on the power consumption.

The basic design approach of a resonator relates to the crystallographic cut (AT, SC ...) and to the overtone to be used.

The SC cut position in the cristalline matrix is discribed on figure 2, and the thermal behavior of an AT cut compared to an SC cut is given on figure 3.

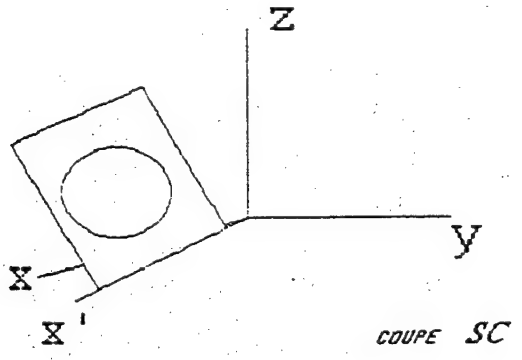
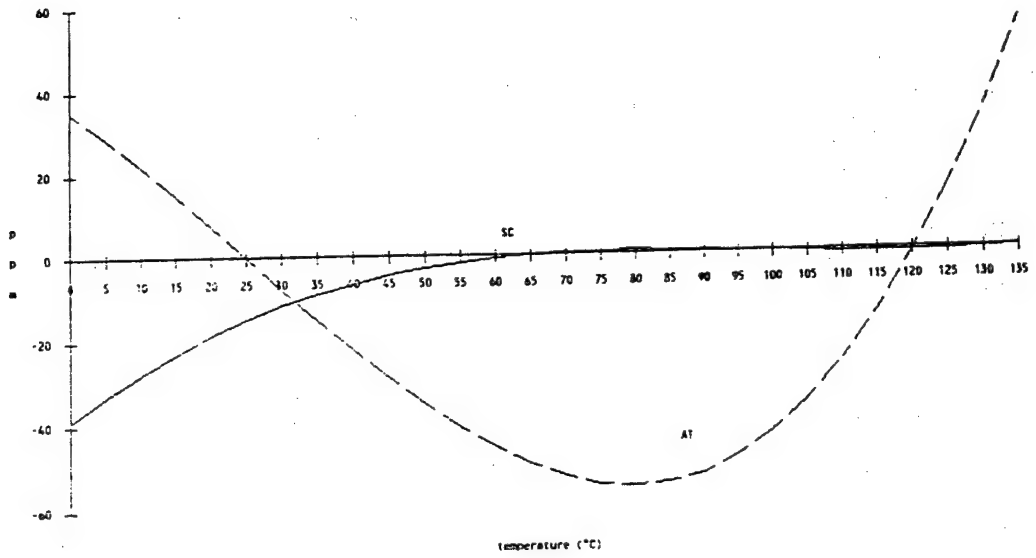


Figure 2

FIGURE 3



When a crystal resonator is placed in an oven, one tries to give to the resonator a F vs T behavior showing a "turn over" temperature arround the oven chamber temperature.

In an oven adjusted to work arround 80 °C, it can be seen that the "radius of curvature" of the F vs T curve of an AT cut is about 10 times larger that the one of an SC cut at the same temperature.

Then, frequency vs temperature will show a better stability with an SC cut than with an At cut.

Moreover, because of the so called "thermal dynamic behavior" of a resonator, which gives the relationship between frequency and the temperature variation with time (df/f (t,T) - â * dT/dt), the warm up characteristic will be significantly better with an SC cut rather than with an AT cut.

SC cut has been selected for GSM oscillators.

Ageing is strongly related to the resonator either through the technology (clean process, know how...) and through the choise of the overtone mode.

Depending of the exact ageing specification, fundamental mode or 3rd overtone can be used. Because of the size of the resonator, fundamental mode have to be choosen for the smallest oscillator (type 2) we are presenting.

The oscillator must be very accutately designed. The main criteria are

- loaded Q factor, related to phase noise close to the carrier
- phase sensitivity vs temperature and time
- supply voltage sensitivity
- drive level sensibility
- harmonic generation

Non linear analysis was used to optimise the oscillator network.

The output amplifier have to be designed along with specific criteria :

- good protection against load variation
- low thermal sensitivity
- high selectivity
- low noise

Classical networks such as common emitter or common base single transistor stages can be used.

Best compromise is to be adjusted between the kind, number of stages, surface on the PCB and cost. This optimisation found different solutions on the three oscillators we are presenting.

The oven construction needs very sophisticated thermal analysis. First of all, the equivallent thermal network parameters have to be determined as an input to the determination of the PID loop, and the thermal behavior have to be optimised regarding thermal properties such as temperature distribution in the structure, thermal leak ways, temperature drift between sensor and resonator..., within extreme conditions of external temperature and heat dissipated on the oven.

Finite element thermal analysis was used to determine basic rules regarding the design of small size / low power ovens.

The network used to drive the power heating transistors from the thermal response of the sensor (generally a thermistor), must control either gain and phase of the correction signal. Various networks can be used to achieve this fonction. The best compromise we found, regarding accuracy, size and cost, is a PID (Proportionnal, Integrator, Derivator) thermal loop.

The last critical part in an oscillator design deals with the voltage regulator. Usually, the oscillator must exhibit performances in various DC external voltage supply variations. Then the oscillator must be protected against these external perturbation. The "filter" is the voltage regulator used to supply the internal oscillator. Natural sensitivity of the "internal" oscillator is in the range of 10^{-7} per volts. To garranty a frequency variation better than 10^{-9} per volt, the voltage regulator must exhibit a DC output stability better than 10 mV.

EXPERIMENTAL RESULTS

The figures N° 4 to 14 give typical results obtain with the oscillators of the PMP, type 1 and type 2 families.

Figures 4 to 7 are related to a PMT type oscillator, whose dimensions are 51*41*25 mm^3.

Figure 4 gives the summary of all the measurements performed on this oscillator.

C.E.P.E — STATEMENT OF MEASURE — Date 29/8/90

S.T.P — No PILOTE : 1PBD F77047

1) Frequency : 16 384 000 Hz

2) Frequency stability as a function of environment

- 2.1) Temperature (-30°C a +70°C) : 5.10^{-10}
- 2.2) Supply voltage 12V ± 10% : $< 1.10^{-10}$
- 2.3) Load (50Ω ± 10%) : $< 1.10^{-10}$

3) Frequency adjustement :

- 3.1) By external trimmer or by positive voltage (1.7 V) : $\pm 1,1510^{-7}$ $-1,5210^{-7}$
- 3.2) Voltage for nominal frequency : 3,7V

4) Current consumption :

- 4.1) Turn on a 25°C during the warm up : 530 mA
- 4.2) Steady state at +25°C : 105 mA

5) Output signal level / 50Ω : 10 dBm

6) Frequency stability as function of time :

- 6.1) Short terme Y (1 Second) : $< 2 10^{-12}$
- 6.2) By day after 96 hours on time : $-1,2\ 10^{-10}$
- 6.3) By year after 30 days on continuous operation :

7) Relative frequency stability after a prior 24 hours turn off

- 7.1) After 30 minutes at -30°C : $+2,610^{-9}$
- 7.2) After 60 minutes at +25°C : $+2,510^{-9}$
- 7.3) Warm up time at -30°C : 7,5 mn

Fig. 4

Figure 5 gives the frequency versus temperature drift in the range -30, 70 °C. The observed stability is better than 5 10^{-10}, to be compared to the spec limit of +/- 1 10^{-8}.

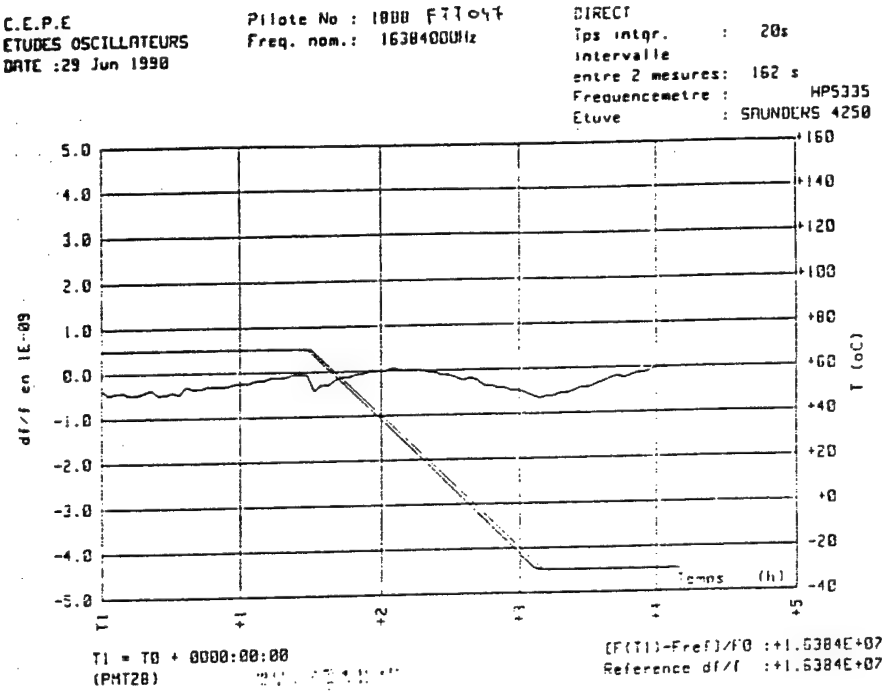


Fig. 5

Figure 6 gives the ageing results of this oscillator. The frequency of the oscillator is measured every day and the frequency drift is plotted on the curve. From this curve, the monthly ageing is better than 4 10^{-9}, (spec limit : +/- 1 10^{-8} per month).

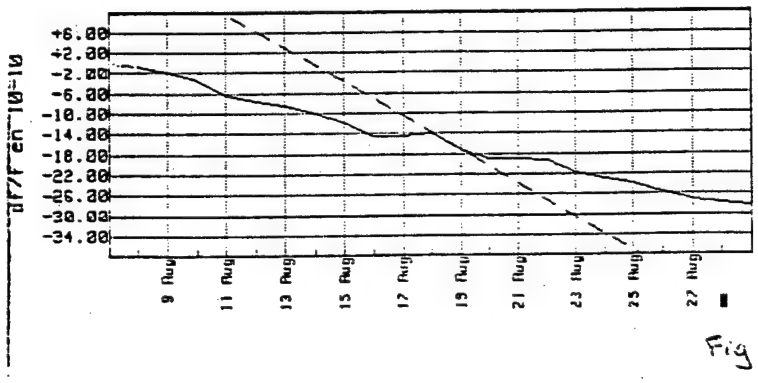


Fig. 6

Figure 7 gives the spectral density of phase fluctuation. The classical form, proportionnal to f^{-3} is observed between 0.1 and 10 Hz, to f^{-1} between 10 and 200 Hz, and a noise floor better than -155 dBc/Hz is obtained for frequencies farther than 1 kHz offset from the carrier.

CEPE
THOMSON-CSF
ST PILOTES
44,av de la Glaciere
95100 ARGENTEUIL (FRANCE)

MESURE OSCILLATEUR PIEZOELECTRIQUE

Date :07/06/1990 STP :
Type :PMT Code :14
Freq.:16.384000 MHz
Freq. FB :.1Hz Freq. FH :100000Hz
INERTE

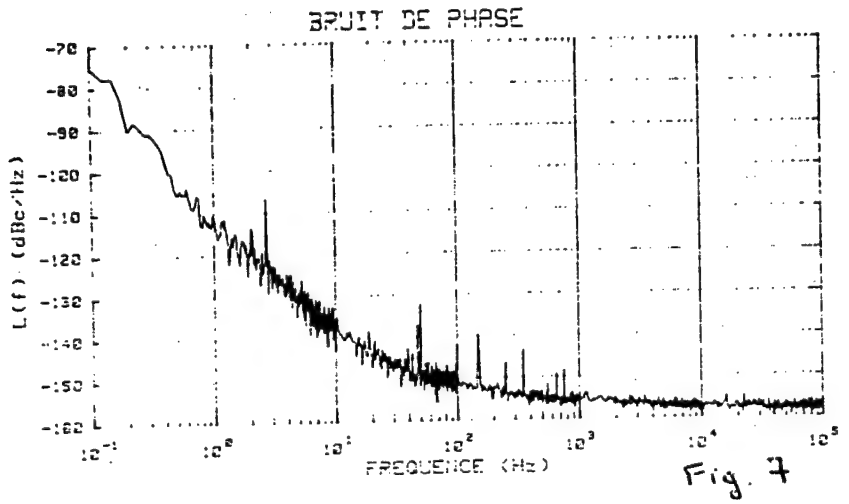


Fig. 7

Figures 8 to 11 are related to a type 1 GSM oscillator, whose dimensions are 40*30*19 mm^3.

Figure 8 gives the summary of all the measurements performed on this oscillator.

STATEMENT OF MEASUREMENT

STP :
Fo : 13 MHz
N° : F 8 F 4 15

			Specification	Measurement
1/	Frequency stability as function of environment			
	1.1/ Temperature range (- 10°C, 70°C)	:	≤ ± 1.10-6	$1,1\,10^{-6}$ p.p.
	1.2/ Supply voltage (12 V ± 10%)	:	≤ ± 1.10-9	$5\,10^{-10}$ p.p.
	1.3/ After warm up in the temperature range	:	≤ ± 5.10-8	$8\,10^{-10}$ p.p.
2/	Current consumption			
	2.1/ During the warm up	:	≤ 400 mA	385 mA
	2.2/ Steady state at 25°C	:	≤ 120 mA	110 mA
	2.3/ Steady state in temperature range	:	≤ 250 mA	210 mA
3/	Output signal			
	3.1/ Shape	:	Square wave TTL compatible.	
	3.2/ Symetry	:	47/53%	50,5 %
4/	Oven alarm	:	VOH when OK VOL when oven is broken	
5/	Aging			
	5.1/ Per month	:	≤ ± 8.10-9	$-7,5\,10^{-9}$
6/	Phase noise	:	See curve	
7/	Frequency adjustment	:	≥ 1.10-6	$1,5\,10^{-6}$

Fig. 8

Figure 9 gives the frequency versus temperature drift in the range -10, 70 °C. The observed stability is better than 5 10^{-9}, to be compared to the spec limit of +/- 1 10^{-8}.

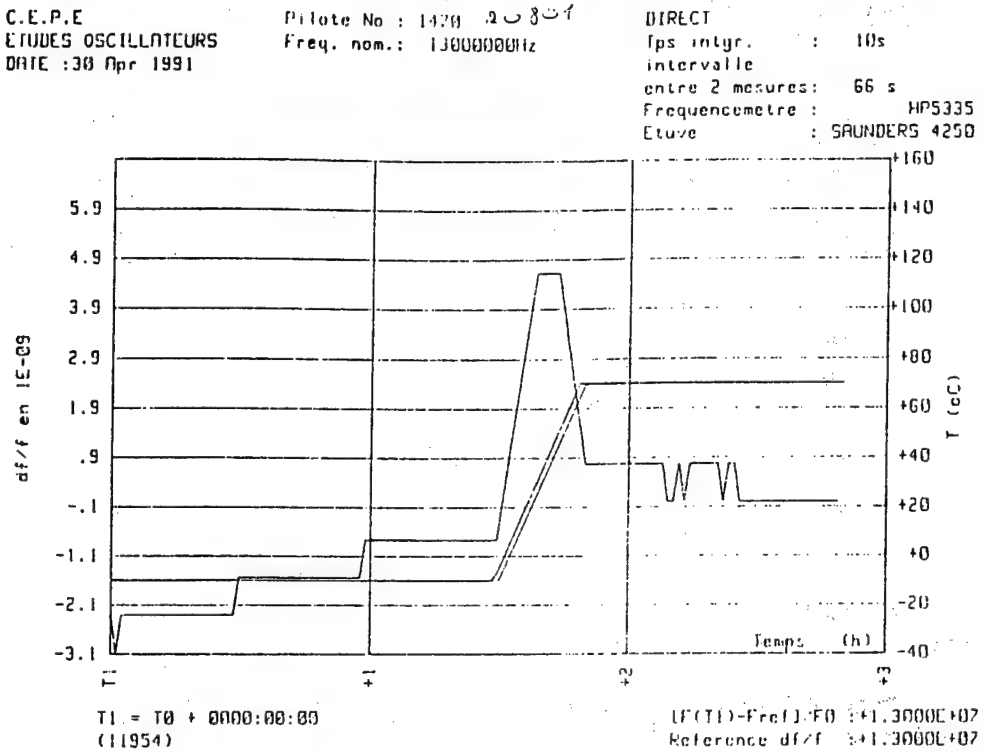


Figure 10 gives the ageing results of this oscillator. From this curve, the monthly ageing is better than 8 10^{-9}.

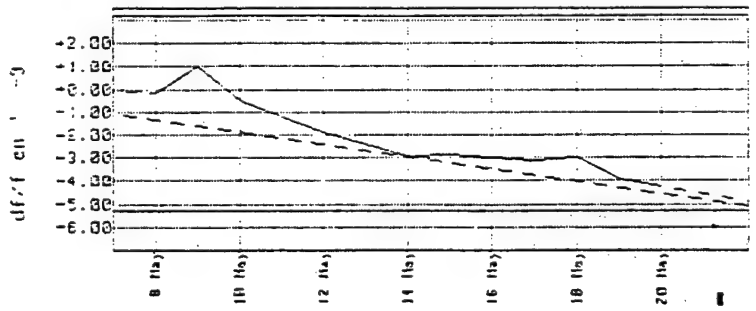


Fig 10

Figure 11 gives the spectral density of phase fluctuation. The classical form, proportionnal to f^{-3} is observed between 0.1 and 10 Hz, to f^{-1} between 10 and 200 Hz, and a noise floor better than -155 dBc/Hz is obtained for frequencies farther than 1 kHz offset from the carrier.

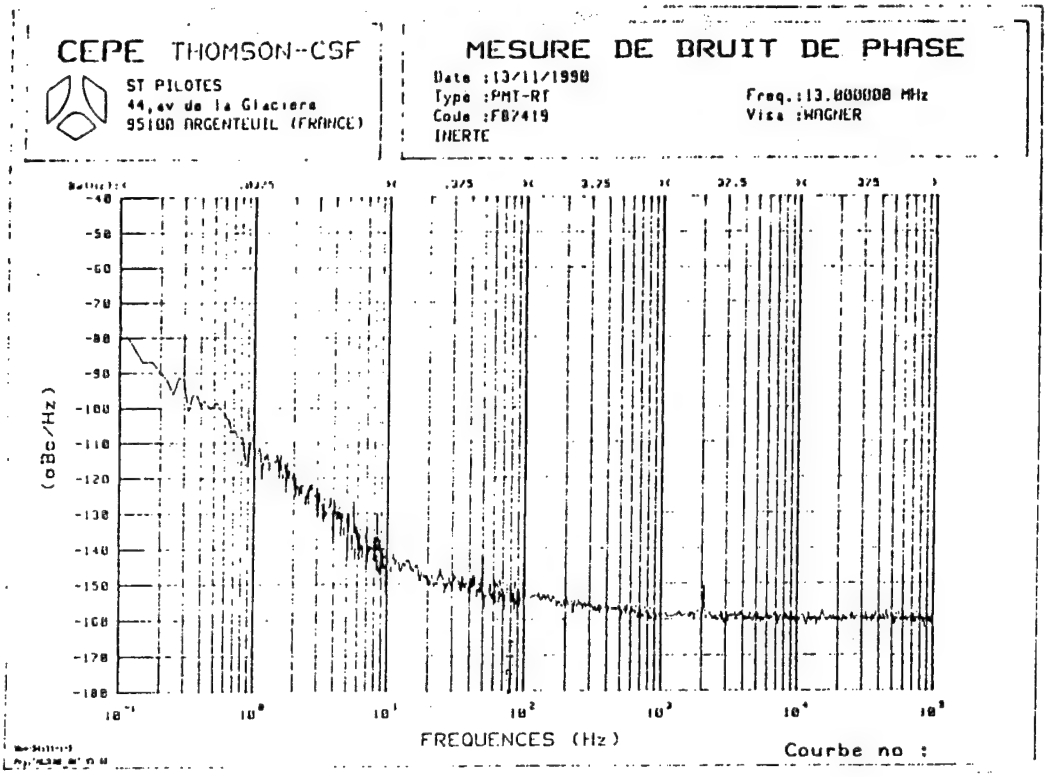


Fig 11

Figures 12 to 14 are related to a type2 GSM oscillator, whose dimensions are 40*30*16 mm^3.

Figure 12 gives the summary of all the measurements performed on this oscillator.

STATEMENT OF MEASUREMENT
TYPE :
FO : 10 MHz
N° : F 76593

1./ FREQUENCY STABILITY AS A FUNCTION OF OPERATING CONDITIONS
- 1.1./ Temperature range (-10°C to + 70°C) : $\pm$ 1 10^{-8}
- 1.2./ Power supply 12 V ± 10% : < $1 10^{-9}$ p.p.
- 1.3./ Load (1 to 2 HCMOS LOADS) : < $1 10^{-9}$ p.p.

2./ OUTPUT SIGNAL
- 2.1./ Wave form : HCMOS Compatibility
- 2.2./ Duty factor : 48 %

3./ WARM UP
- 3.1./ After 2 mn switch on at 25°C : $4,3 10^{-8}$
- 3.2./ After 5 mn switch on at 25°C : $1,3 10^{-8}$
- 3.3./ After 5 mn switch on at - 10°C : $1 10^{-8}$

4./ CURRENT CONSUMPTION
- 4.1./ During warm up : 640 mA
- 4.2./ Steady state 25°C : 120 mA
- 4.3./ Alarm level — Steady state : VOH HCMOS; Warm up (5 mn max) : VOL HCMOS

5./ FREQUENCY ADJUSTMENT
- 5.1./ By external potentiometer : $+1,6 10^{-6}$ / $-3,5 10^{-6}$

6./ LONG TERM FREQUENCY STABILITY
- 6.1./ Per day : $2,27 10^{-10}$
- 6.2./ Per month : $\pm$ $6,7 10^{-9}$

7./ PHASE NOISE
- 7.1./ At 1 KHz : - 150 dBc/Hz
- 7.2./ At 10 KHz : - 150 dBc/Hz

8./ STABILIZATION TIME AFTER A SHORT INTERRUPTION OF EQUAL TO 2 MINUTES AT - 10°C
- $\pm$ 2.6.10^{-6} : 30"
- $\pm$ 2.6.10^{-7} : 2'

Fig 12

Figure 13 gives the frequency versus temperature drift in the range - 10, 70 °C. The observed stability is better than 3 10^{-8}, to be compared to the spec limit of +/- 1 10^{-7}.

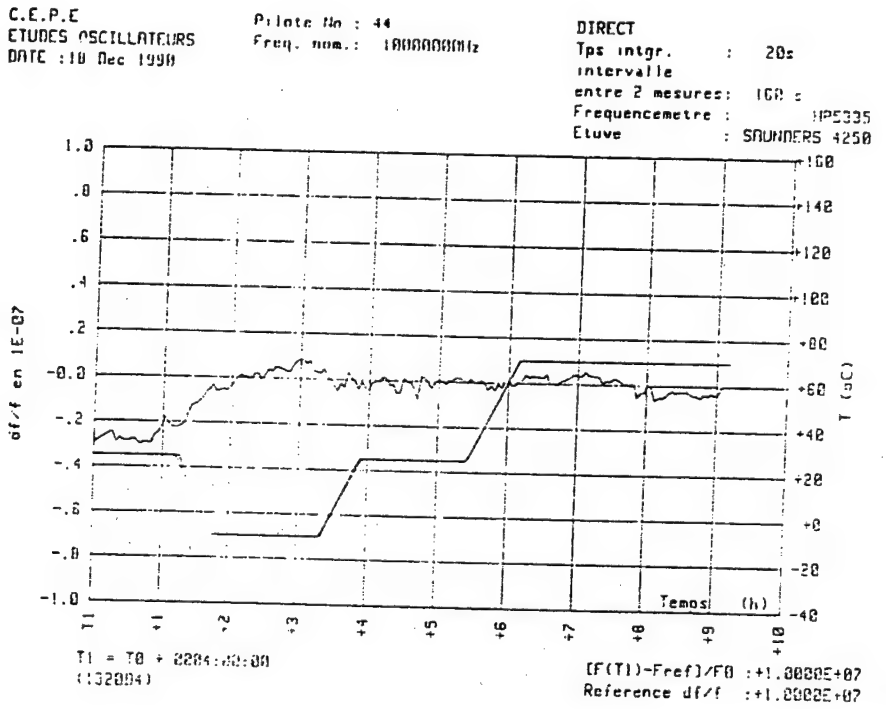


Fig 13

Figure 14 gives the ageing results of this oscillator. From this curve, the monthly ageing is better than 8 10^{-9}, (spec limit : +/- 3 10^{-8} per month).

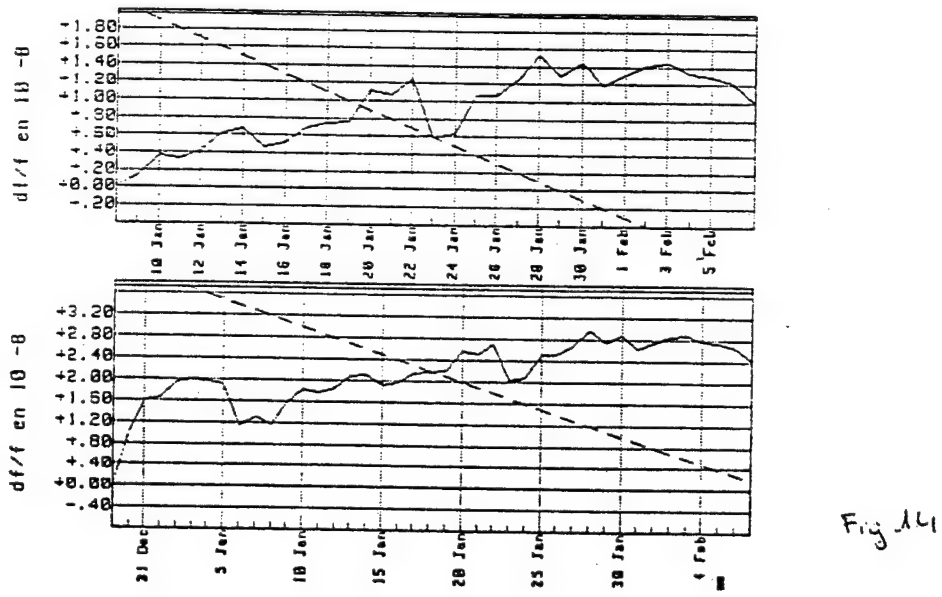


Fig 14

Figure 15 gives the spectral density of phase fluctuation. The spectrum proportionnal to f^{-3} is observed between 0.1 and 10 Hz, to f^{-1} between 10 and 200 Hz, and a noise floor better than -145 dBc/Hz is obtained for frequencies farther than 1 kHz offset from the carrier.

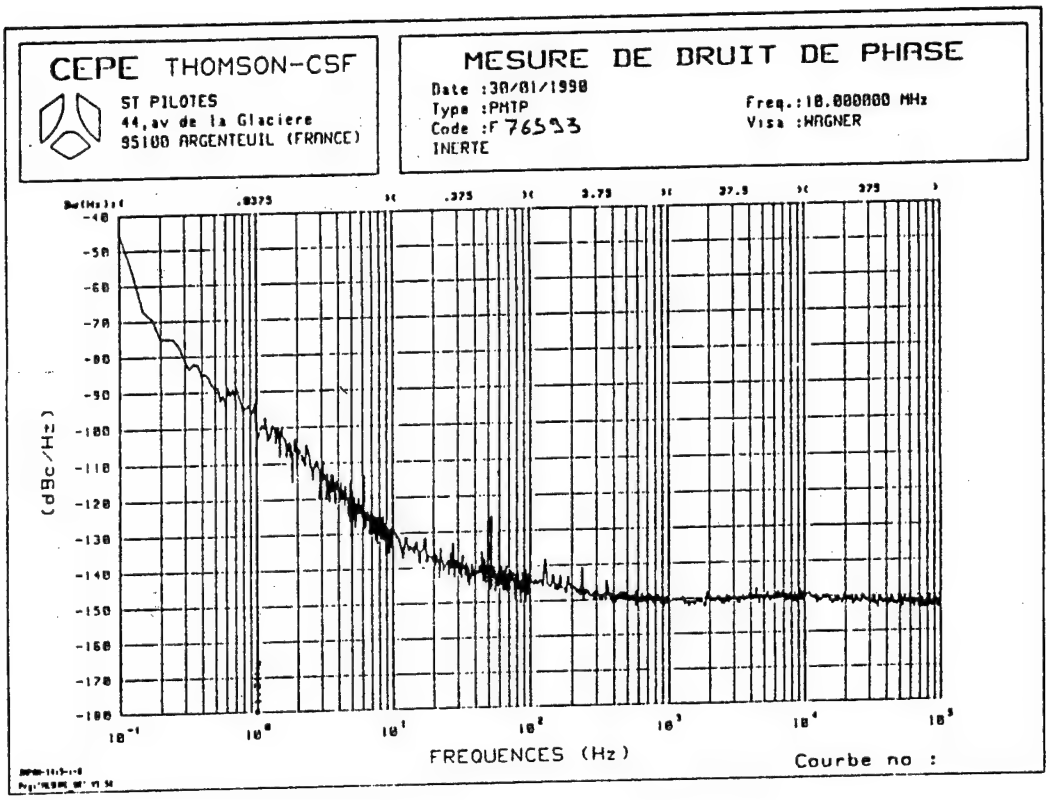


Fig 15

QUALIFICATION

These oscillators have been submitted to a qualification procedure agreed with customers.

The qualification tests sequence generaly used is as followed :

pre ageing (< 2 months)
initial electrical measurements
humidity
thermal shocks
mechanical shocks
solderability and solder heat resistance
visual inspection
evaluation of ageing enhancement vs natural
final electrical measurements

The initial and final electrical measurements cover :

* short term stability
* power consumption — during warm up
  steady state at 25 °C
* electrical tuning — nominal
  adjustment range
* output power
* harmonics / non harmonics spuriousses
* Frequency sensibility versus load
  DC voltage supply
* Frequency variation in temperature range
* Warm up after turn off :
  frequency after "x" time after turn on
  time to within "y" 10^{-6} after turn on

The electrical conformity is checked in comparison of each oscillator specification.

CONCLUSION

The GSM ground base oscillator specifications can be met when using state of the art of oscillators design and manufacture concepts. Design to cost and design to manufacturability approaches have prooved to be powerfull tools when working on high technical devices to the professionnal market.

The experimental and statistical results show that the GSM requirements are obtained with very good oscillators yields.

LIQUID HEAT SINK, A NOVEL APPROACH FOR ENHANCED COOLING OF MICROELECTRONICS

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I) ABSTRACT

The continual drive for smaller and denser microelectronic packages makes cooling a tough engineering problem.
In some cases, heat fluxes beyond the cooling capabilities of forced air cooling occur. Immersion cooling with a dielectric liquid is the solution. A drawback of liquid immersion cooling is the design of a complex liquid handling system.
For applications in the range between forced air cooling and liquid immersion cooling, there is a solution available now which offers the advantages of direct contact cooling with dielectric liquids without having to deal with liquid containment.

This novel approach is called the liquid heat sink. It consists of a plastic pouch, completely filled with a fluorocarbon liquid. The liquid heat sink occupies the space between the electronics and outside walls of the cabinet in which the electronics are housed. The liquid heat sink transfers the heat from the components to the cold plate or the container walls.

II) TRENDS IN MICROELECTRONICS

New developments in microelectronics require the development of new approaches in thermal management. (1) The following paragraphs highlight some of the microelectronic developments.

Integrated circuit die sizes will be increased from approximately one square centimeter to two square centimeters by the year 2000. X-ray or ion beam technology is projected to permit feature sizes to shrink from approximately one micron to one tenth of a micron by the year 2000. (Fig. 1)

Increases in the chip circuit density are the result of the smaller feature sizes being produced. For DRAM (Dynamic Random Access Memory) devices, the chip density is projected to be approximately 1E+07 bits per chip in the late 1990's. CMOS (Complementary Metal Oxide Semiconductor) and bipolar logic devices, although lagging the DRAM devices by 2-5 years, are also projected to increase in density. (Fig. 2).

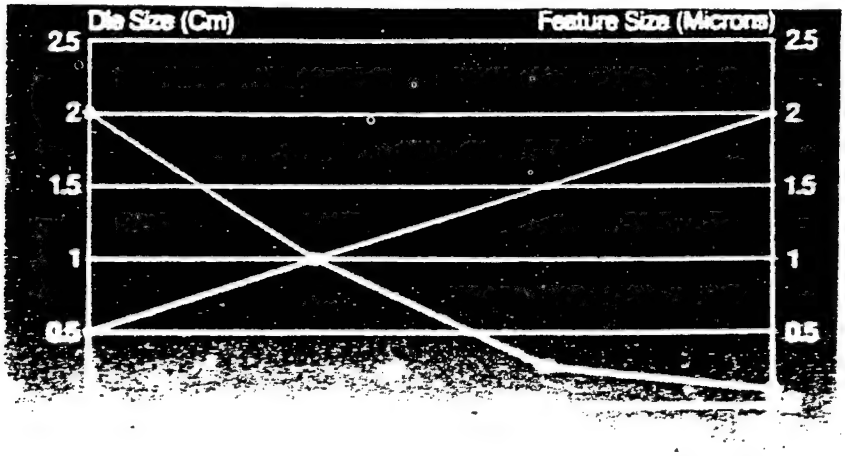


Figure 1. IC dies size trends

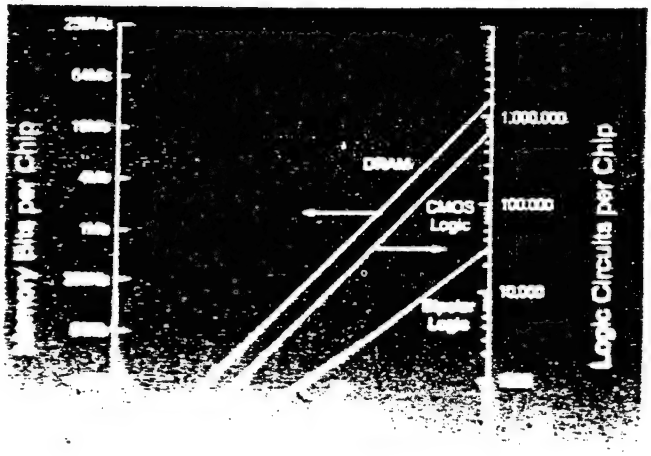


Figure 2. Chip density trends.

Switching speeds are dropping dramatically. Conventional devices are projected to converge to fifty picoseconds switching speed by the year 2000. Josephson devices are projected to have switching speeds of one picosecond by 1995. The CRAY-2, using ECL (Emitter Coupled Logic) technology, has an in-chip propagation delay of approximately three hundred fifty picoseconds. The CRAY-3 (2), using GaAs technology for the logic devices is reported to have a chip propagation delay of less than eighty picoseconds. (Fig. 3).

If the thermal management system is not improved, the component temperatures will start rising.

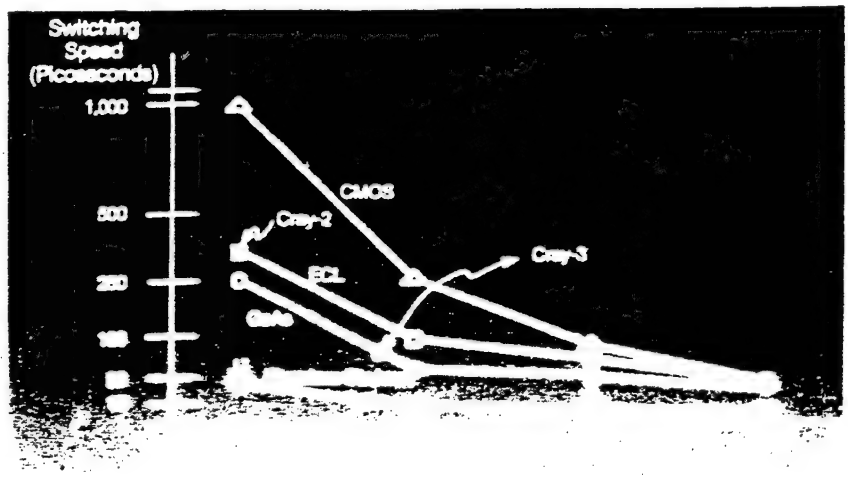


Figure 3: Switching speeds

The failure rate of IC's (Integrated Circuits) is dependent on temperature. Fig. 4 shows the acceleration in failure rate as a function of the temperature. In this case the failure rate doubles for a 10°C temperature rise. This demonstrates the importance of operating at the lowest possible temperature to increase the reliability of electronics (3).

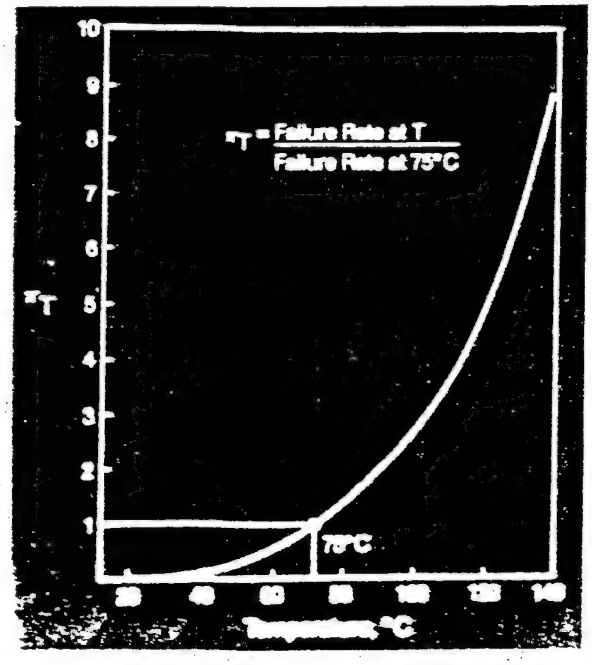


Figure 4. Thermal acceleration of failure rate

III) DESCRIPTION OF THE LIQUID HEAT SINK

The liquid heat sink consists of a plastic pouch, completely filled with a perfluorocarbon liquid, and is used as a heat transfer vessel with a standard thickness of 3.15 millimeters. The pouch is closed by impulse heat sealing. Several tests are made on the pouch, to assure quality and reliability.

1) The plastic film

The pouch is comprised of 4 layers of plastic film with an overall thickness of 0.15 millimeters. The 4 components from inside to outside are chosen for :

* excellent heat sealability,
* good mechanical strength,
* gas and liquid barrier properties,
* flame retardancy

The thermal conductivity of the plastic material is measured to be k_{film} = 0.231 Watts/meter . centigrade, according to method ASTM F-433.

2) The perfluorocarbon liquid

The liquid used to fill the pouch is FLUORINERT (TM) Electronic Liquid.

The FLUORINERT (TM) Liquids are members of a family of completely fluorinated organic compounds that have a unique combination of properties. They are derived from common organic compounds by replacement of all carbon-bound hydrogen atoms with fluorine atoms. Fluorocarbon compounds can be perfluoroalkanes, perfluorotertiary amines and perfluoropolyethers.

Since fluorination of the organic compound is complete, the products contain no hydrogen or chlorine. This makes the properties of the fluorocarbon liquids vastly different from hydrocarbons or chlorofluorocarbons (commonly used as degreasing solvents, refrigerants and aerosol propellents).

The FLUORINERT (TM) Liquids are extremely non-polar and have esentially no solvent action. They are colorless, odorless, low in toxicity, and non-flammable. They also have high thermal stability, low chemical reactivity, and leave essentially no residue. Their non-polar character leads to many of their unusual physical properties, such as low heat of vaporization, low surface tension, and low boiling point in relation to their high molecular weights. Some of the physical properties of the fluorocarbon liquids are shown in Table 1. (4)

When looking at heat transfer equations, one can see the heat transfer coefficient can be maximized with :-

* high density, heat capacity and expansion
* low viscosity

TABLE 1
Typical fluorocarbon cooling liquids properties, compared to other heat transfer media.

	Water	Fluorocarbon Liquid	Silicone Oil	Air
ρ, density Kg/ cubic m	998	1592	950	1.099
β, coef of exp 1/K	4.86 E-04	.0016	.0010	.0031
μ, viscosity Kg/m*s	5.47 E-04	4.78 E-04	2.85 E-02	1.85 E-05
c, specific heat J/Kg*K	4186	1046	1629	1046
K, thermal conductivity W/m*K	.683	.054	.156	.03
σ, surface tension N/m	.068	.0085	.021	N/A
h , heat of vaporization J/Kg	2.26 E+06	8.79 E-04	N/A	N/A
Dielectric strength KV/0.1"	N/A	38	-	-

Fig. 5 compares the heat transfer coefficients of different cooling techniques.

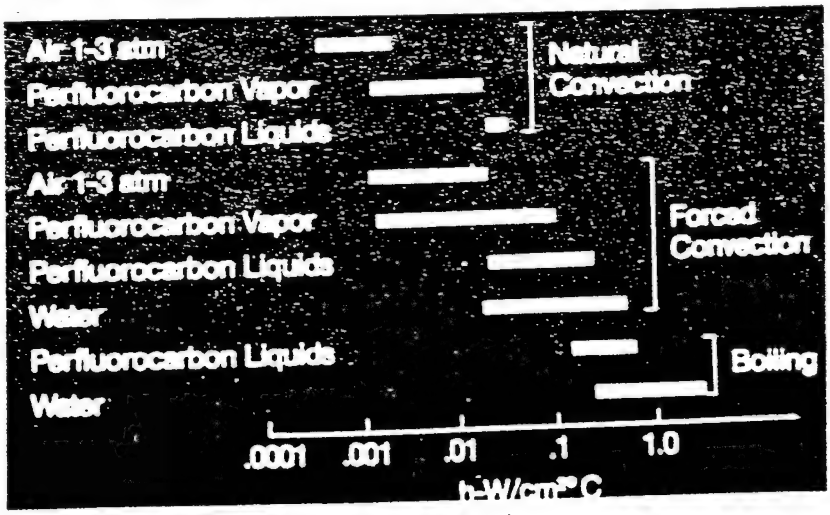


Figure 5.

3) The liquid heat sink (5)(6)

The plastic pouch is filled with perfluorocarbon liquid and then degassed to prevent the introduction of gas bubbles during use in the electronic assembly. The current maximum operating temperarure of the bag is 80°C. This maximum use temperature is set by film properties and seal strengths. In actual use, the liquid heat sink should be sandwiched between the electronic components and a cold plate with a minimum contact pressure of 7000 Pascal to maximize the heat transfer.
This cold plate can be the cabinet wall or a planar heat exchanger.

IV) THERMAL PROPERTIES OF STANDARD VESSELS (7)(8)

In 3M's laboratory, the thermal properties of the liquid heat sink have been tested by measuring the thermal resistance of a standard thickness liquid heat sink as a function of surface area, temperature difference, and heat transfer direction at a contact pressure of 7000 Pascal. The actual experimental set-up of testing is shown in Fig. 6. The thermal properties of the liquid heat sink are measured by monitoring the temperature difference over the bag.

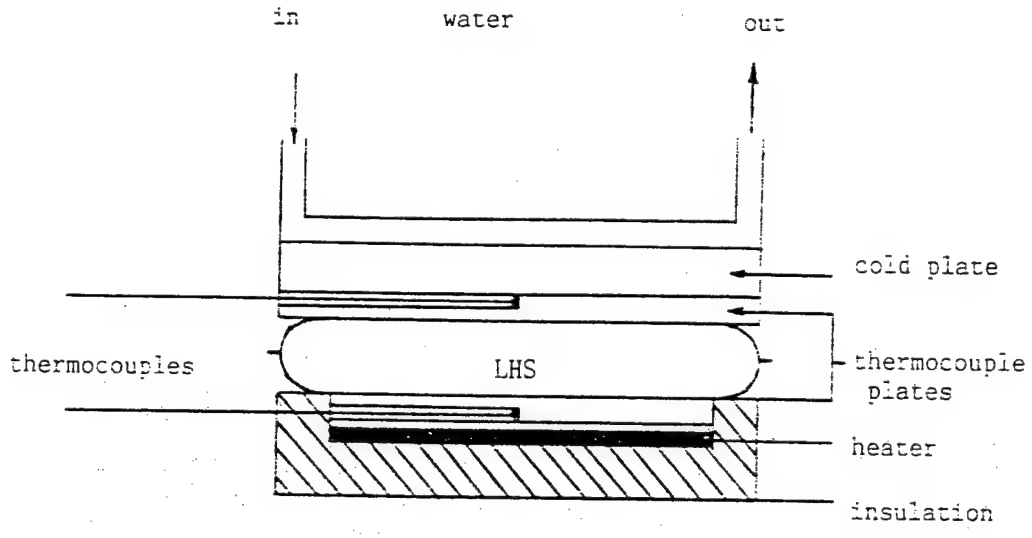
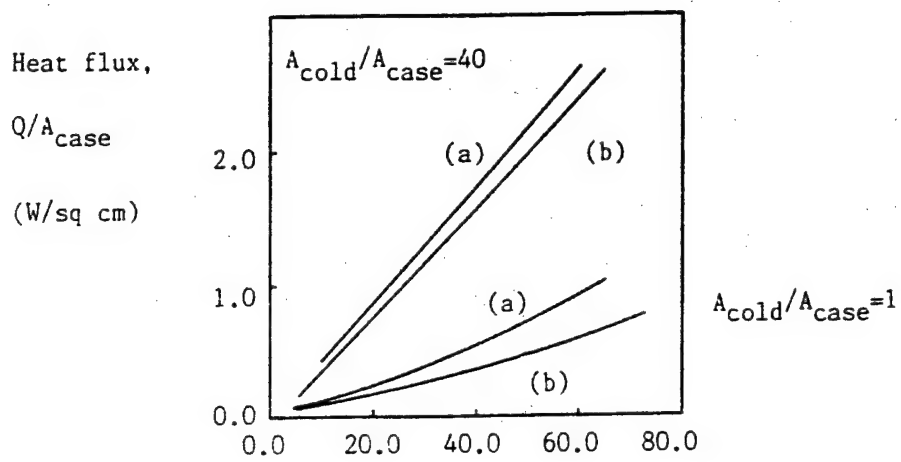


Fig. 6. Experimental apparatus

Heat transfer through the liquid heat sink is a function of the temperature difference between the device case and the cold plate ($T_{case} - T_{cold}$) the orientation of the LHS, and the ratio of cold plate to device area in contact with the LHS (A_{cold}/A_{case}).

The graph at Fig. 7 summarizes experimental data collected showing heat flux through the LHS as a function of ($T_{case} - T_{cold}$) and orientation. The heat flux on the vertical axis is expressed in Watts per square centimeter based on the device case area in contact with the LHS (Q/A_{case}).



(a) horizontal orientation
(b) vertical orientation

Fig. 7. Heat transfer measurement

The lower pair of lines in this graph represent data collected for a liquid heat sink between a heat source and cold plate of equal areas (A_{cold}/A_{case} = 1). The upper pair of lines represent data collected for a small heat source in contact with the LHS and a larger cold plate (A_{cold}/A_{case} = 40).

The increase in local heat flux, Q/A_{case}, for the small heat source is due primarily to the lower average operating temperature of the LHS and the improved conditions for fluid circulation inside the LHS.

In typical applications, several devices will be in contact with a single liquid heat sink and the power level may vary significantly from one device to another. This makes it difficult to accurately predict the heat transfer performance that will result from use of the LHS. However, the graph at Fig. 7 and the empirical equations given below, can be used to estimate a range within which the performance can be expected to fall. Fig. 7 also illustrates the effect of orientation on liquid heat sink performance. The lower pair of lines with A_{cold}/A_{case} = 1 show that the heat flux for a given temperature difference is 70% higher for the horizontal orientation compared with the vertical orientation. This difference is a result of the shorter convection flow path in the fluid for horizontal orientation.

The difference in performance with respect to orientation is much less (approximately 10% in Fig. 7) as the area ratio between the cold plate and the heat producing surface increases. This is probably due to the creation of a shorter convective flow path as illustrated in Fig. 8.

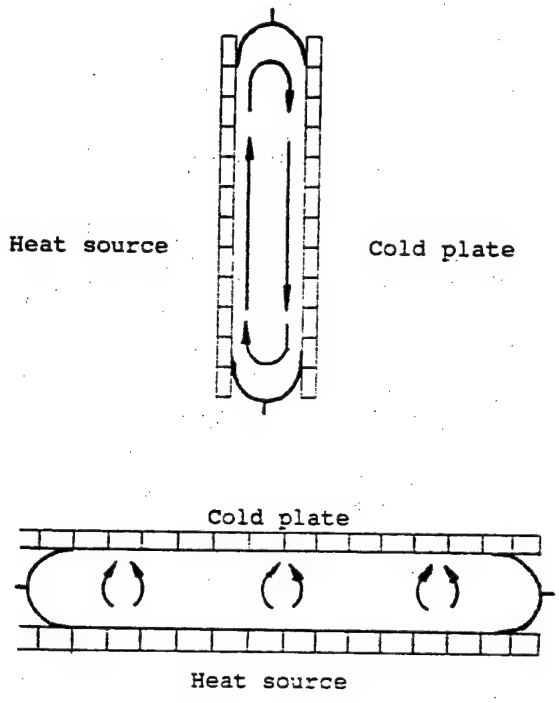


Fig. 8. Effect of orientation on heat transfer medium

Data from the graph at Fig. 7 was used to develop the following equations :

Equation 1 - Horizontal orientation

$$\frac{Q}{A}_{case} = \frac{(T_{case} - T_{cold})^{1.28} (A_{cold}/A_{case})^{0.5}}{184} \qquad (1)$$

Equation 2 - Vertical orientation

$$\frac{Q}{A}_{case} = \frac{(T_{case} - T_{cold})^{1.28} (A_{cold}/A_{case})^{0.5}}{307} \qquad (2)$$

These equations can be used to estimate the thermal performance of the liquid heat sink for the heat flux from the device case up to 3 watts per square centimeter and for temperature differentials ($T_{case} - T_{cold}$) of up to 70°C with less than 15% error.

V) THE EFFECT OF CONTACT PRESSURE ON HEAT TRANSFER

As discussed earlier, the thermal resistance or heat transfer coefficient is dependent on the contact pressure between the liquid heat sink and the electronic components. This has been determined by comparing the heat transfer coefficients at different contact pressures to the heat transfer coefficient measured at 11000 Pascal.
The results of this investigation are shown in Fig. 9.

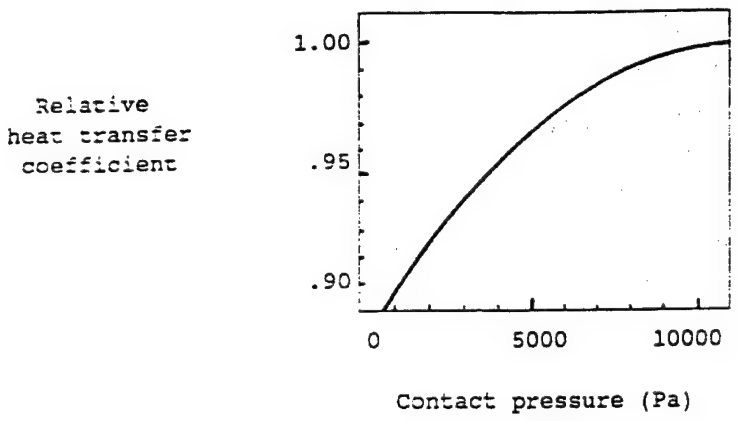


Fig. 9. Effect of contact pressure on heat transfer

It can be seen that the heat transfer coefficient is maximized up to 95% at a minimal contact pressure of 4000 Pascal. A lower pressure, small air gaps between the pouch and the electronic components or the cold plate occur reducing the heat transfer coefficient and increasing the overall thermal resistance.

VI) ADVANTAGES OF A LIQUID HEAT SINK OVER OTHER COOLING TECHNIQUES

- By eliminating air flow across the circuit board, the liquid heat sink will keep the system clean. Dirt and lint brought into an electronic system can lead to long-term reliability problems.

- The presented technique offers passive cooling, eliminating the noise produced by a fan. This system has no moving parts.

- Forced air cooling generally requires wide spacing between circuit boards to obtain adequate air flow distribution. Liquid heat sinks can be used to reduce the physical size of the electronic assembly.

- Unlike some materials used to conduct heat away from a printed circuit board, the liquid heat sink has a flame resistant outer layer.

- The liquid heat sink operates at a fairly uniform temperature. The fluid is constantly circulating in the liquid heat sink during operation and provides a uniform temperature in contact with the circuit board. This can be helpful in systems that operate at high speeds. Temperature differences between devices operating at high speeds can affect their ability to communicate.

- One additional advantage beyond removing heat from the circuit, the liquid heat sink can act as a shock absorber in some applications. (4)

VII) CONCLUSION

The liquid heat sink offers a solution to thermal management problems. The generation presented in this article is able to deal with heat fluxes in the range of forced air cooling, without the concerns present with fans and air flows through a system.

VIII) SYMBOLS, ABBREVIATIONS, AND REFERENCES

A = surface area in L^2

A_{case} = surface area of the device case in contact with the liquid heat sink in cm^2

A_{cold} = surface area of the liquid heat sink

k_{film} = thermal conductivity of the plastic film

q'' = heat flux in W/cm^2

Q = heat in W

T = temperature in °C

T_{case} = temperature of the components in °C

T_{cold} = temperature of the cold plate in °C

ΔT = temperature difference over the LHS in °C

CMOS : Complementary Metal Oxide Semiconductor
DRAM : Dynamic Random Access Memory
GaAs : Gallium Arsenide
ECL : Emitter Coupled Logic
IC : Integrated Circuit
RAM : Random Access Memory

(1) F.P. Incropera, "Liquid Immersion Cooling of Electronic Components". Presented at ICHMT XXth International symposium, Dubrovnik, Yugoslavia, September 1988.

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(6) 3M FLUORINERT (TM) Liquid Heat Sink product manual (1988).

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800 MHZ DIELECTRIC BANDPASS FILTERS FOR MICROCELL DIGITAL CELLULAR BASE STATIONS

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Murata Manufacturing Company, Ltd., Kyoto, JAPAN

Abstract

A novel high power bandpass filter using TM_{110} dual mode dielectric resonators was developed. TM_{110} dual mode is achieved with dielectric resonators physically coupled in an asymmetrically orthogonal manner. These arrayed resonators are constructed in monoblock and have high unloaded Q. By assembling these resonators, a high power bandpass filter in 800MHz was realized. Specific features achieved with this new filter are, very low insertion loss of less than 0.4dB with center frequency of 840MHz and band width of 40MHz, and its small physical size of 80×90×180mm, which corresponds only less than 30% of the conventional type of high power bandpass filter using reentrant cavity resonators. This filter is useful as an antenna filter for FDMA cellular base stations as well as microcell digital cellular base stations.

Introduction

Cellular mobile telecommunication systems are expanding rapidly world wide. For the base station equipments of these systems, high power filter was proposed by applying TM_{110} mode dielectric resonators with high K ceramic material, featuring small size and high efficiency.[1] Some of these filters are in actual operation as antenna filter of FDMA cellular base stations since several years.[2][3] A technology was developed to realize a 4GHz band TM_{110} dual mode dielectric resonator physically coupled in orthogonal manner and arrayed (abbreviated as ASODR hereafter). By using this technology, a 4-section dielectric filter was realized in smaller size, which was applied for an equipment in terrestrial stations of 4GHz band satellite systems.[4]

As microcell systems are being projected, smaller in size, less expensive, and reliable equipments are required for the base stations. To meet this tendency, much smaller, more effective, and highly reliable filter is requested. For this purpose, new technologies were developed, namely a forming technology of full monoblock type TM_{110} dual mode dielectric resonators, and a design technique of multi-section bandpass filter. By utilizing these technologies, a high power, high performance dielectric filter in smaller dimension has been developed for 800MHz band cellular base stations. Electrical performance and construction of 800MHz band ASODR, and construction, design, and performance of filter utilizing ASODR's are described in this paper.

Electrical performance of ASODR

Electric field distribution of TM_{110} dual resonant mode of symmetrically constructed orthogonal dielectric resonator is shown in Fig. 1. Two modes generated are called even

mode and odd mode respectively. The two resonant modes are independent of each other, and electromagnetic coupling is not created, thus no series coupled multi-section filter can be realized. Electric field distribution of asymmetrically constructed orthogonal TM_{110} dual resonant mode is shown in Fig. 2. The dielectric posts are partially removed at the overlapped cross junction. This asymmetric construction causes electrical perturbation between the two modes. The two resonant frequencies created are called f_{even} and f_{odd}, whereas f_{odd} is higher than f_{even}. Comparing with TM_{110} single mode dielectric resonator, degradation of unloaded Q is less than 5%.

The advantage of ASODR is that the degradation of unloaded Q by changing the coupling coefficient(k) is small enough, and thus large k can be realized. Fig. 3 shows the relation between k and unloaded Q. When a conventional metal screw is applied, maximum value of k is about 4%, and unloaded Q is falling down to about a half value. On the other hand, the result of ASODR proves that the maximum k can be more than 10%, and the deviation of unloaded Q is less than 8%. The k value can be controlled easily and stably by the depth of grooves at the cross junction of resonator posts. Fig. 4 shows the relation between k and d/D. Experimental relation is represented by following equation.

$$k = 2.0\times(f_{odd}-f_{even})/(f_{odd}+f_{even}) = 0.281\times(d/D+0.4)^{1.585}$$

Design parameter can be calculated by using this equation.

Construction of ASODR and filter

A full monoblock TM_{110} dual mode ASODR in 800MHz band was developed, construction of which is shown in Fig. 5. Dielectric material is $(Zr\cdot Sn)TiO_4$, with dielectric constant of 38, dielectric loss tangent of 4.0×10^{-5} at 800MHz band, and temperature coefficient of about 0.6 ppm/°C. TM_{110} dielectric resonator posts and frames are formed in full monoblock, which is the particular feature improved from the former result of ASODR in 4GHz band. Thus the productivity could be drastically improved compared with the conventional hand assembly of resonators with frames. The electrode on the outer shell is fired silver. Resonant frequency can be tuned by high K dielectric rod very easily and linearly. Coupling constant is controlled by the design of the grooves at the cross junction of the resonator posts. ASODR in 800MHz band has unloaded Q of about 3000, and outer dimension of 60x60x50mm. The outer shell with dielectric frames results in little degradation of electrical performance, evidenced by the deviation of the resonant frequency of less than 2%, and the degradation of unloaded Q of less than 7% compared to those with solid metal shell. The well-known problem of contacting dielectric resonator posts steadfastly with the metal frames is solved by the full monoblock construction.

Basic construction of high power bandpass filter in 800MHz band is shown on Fig. 6. In the last ASODR filter in 4GHz band, only one ASODR with two TM_{110} single mode dielectric resonators are applied to realize a 4-section filter. This time, filter design technique has been improved, and a 6-section filter can be realized by using only 3 ASODR's. Obviously the number of resonator blocks required for a filter can be reduced down to a half by applying ASODR's, thus contributing to further size reduction.

Coupling between the ASODR's can be realized by conductive slitted silver plated ceramic fins, and by the spacing of the fins. This fin enables selective coupling of only one

directional pair of TM_{110} dual mode of ASODR's arrayed in series. Coupling of the resonators with external loads of input/output are realized by coupling coils, which are adjusted to couple only with one directional resonant mode. Outer electrode of ASODR is grounded, and resonator is grounded by soldering through meshed metal foil.

These are the key technologies, based on which a bandpass filter composed solely of ASODR's has been materialized. The filter is mounted in a metal housing to assure the positioning of the resonators. This construction guarantees high stability against mechanical shock and high reliability in the specified ambient temperature and humidity.

Filter design

Equivalent circuit of the filter is shown in Fig. 7. The value of filter design parameters are determined by the design technique of conventional Chebysheff pass band characteristics. The resonant frequency of each resonator can be tuned by inserting dielectric rod. Tuning range is about 8MHz, and frequency shift is proportional to insertion length of the rod, consequently tuning is very easy. Unloaded Q of the resonator will not be degraded by this tuning procedure. Since coupling between the resonators are designed precisely, the coupling constant must be adjusted very accurately. Coupling of external Q is adjusted by the shape and size of the loop coupling probes.

Energy loss at each dielectric resonator is calculated at 1.4 Watts maximum during a total input power of 70 Watts. Temperature rise by the loss at each dielectric resonator is calculated by numerical analysis, and this value with ASODR construction is suppressed to less than 10 degrees. Fig. 8 presents analytical results of temperature distribution of ASODR, which proves that the degradation of filter characteristic is minimum.

When two input signals with different frequencies have power level of 30 Watts, electric field intensity in dielectric resonators is calculated to be 17 V/mm maximum by using FEM technique. Under this condition, experimental measuring results exhibits that the level of third order intermodulation is suppressed to less than −150dBc, which is low enough to cause any negative influence in the receiver band.

Performance of the filter

A prototype of a bandpass filter in 800MHz band was realized by applying ASODR's only. Performance of the filter is shown in Table 1. The filter has 6-section construction, with center frequency of 840MHz, pass band width of 40MHz, insertion loss of less than 0.4dB over the whole pass band, and return loss of more than 22dB in the pass band. Attenuation at $f_0 \pm 60$MHz measures more than 46dB. Frequency response of attenuation and return loss are presented in Fig. 9. It shows good agreement between calculated curve and obtained one.

Operating temperature range is between −10°C and +60°C, and humidity range is 20 to 80%. Frequency stability is about 1ppm/°C, and the drift of center frequency is about 30kHz.

While input power is 70 Watts, temperature rise in the resonators is about 9°C, which coincides well with the calculated value. Measured temperature distribution in ASODR is shown in Fig. 10. Maximum input power can be up to 500 Watts. Measured value of third

order intermodulation is less than -150dBc.

Physical size is 80x90x180mm, which corresponds to about a half of dielectric filter applying only TM_{110} single mode resonators, and about a quarter of conventional filter with reentrant cavity resonators. Thus a great deal of size reduction was realized.(cf. Table 2) The filter weigns about 3.0kg, and can be handled easily. Mechanical shock of 50G maximum does not exert any adverse affects on filter characteristics.

These results shows successfully good practical performance and reliability. Outlook of this filter is shown in Fig. 11.

Conclusion

Full monoblock construction of TM_{110} dual mode dielectric resonator(ASODR) has been realized with unloaded Q of 8000 minimum. A filter design technique was developed to apply soleiy ASODR's, to realize a 6-section high power bandpass filter with only 3 ASODR's. Finally, a new bandpass filter was developed by applying ASODR's, featuring small size and high reliability during high power operation. The filter has center frequency of 840MHz, with insertion loss of less than 0.4dB, return loss of more than 22dB. During the input power of 70 Watts, the temperature rise is less than 10°C, and intermodulation level is less than -150dBc. The physical dimension is 80x90x180mm, which corresponds only a quarter of what has been realized by reentrant air cavity resonators.

By the technologies described, a high power bandpass filter could be realized in smaller dimensions with promised productivity. This filter is useful as antenna filter especially for the microcell operation, which is said to be one of the significant aspects of the coming digital cellular services.

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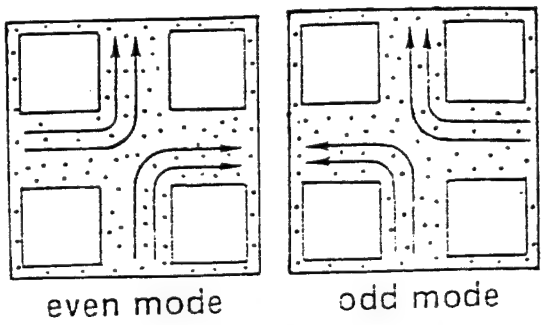

Fig.1 Electric field distribution of symmetrically constructed orthogonal dielectric TM_{110} dual resonant mode

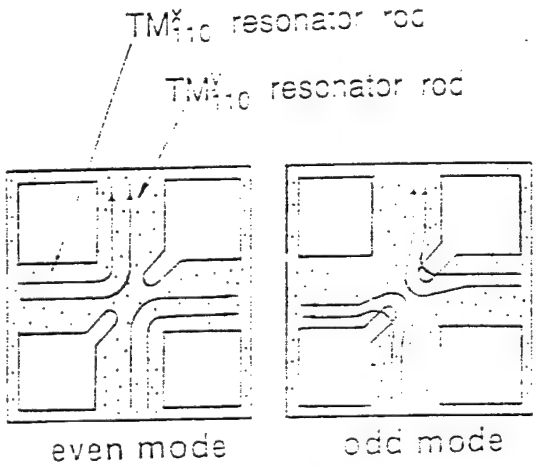

Fig.2 Electric field distribution of asymmetrically constructed orthogonal dielectric TM_{110} dual resonant mode

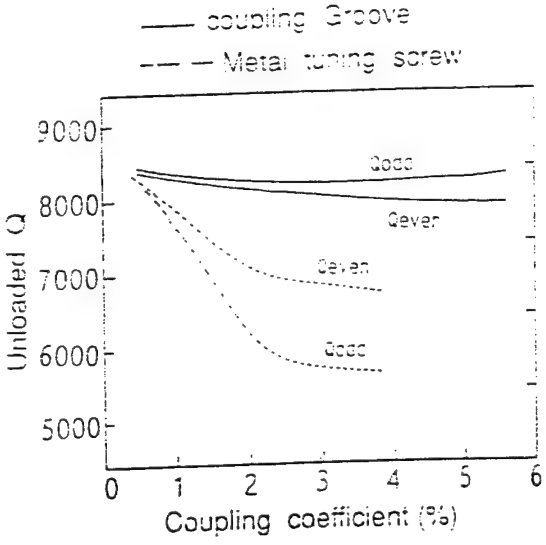

Fig.3 Relation between coupling coefficient and unloaded Q

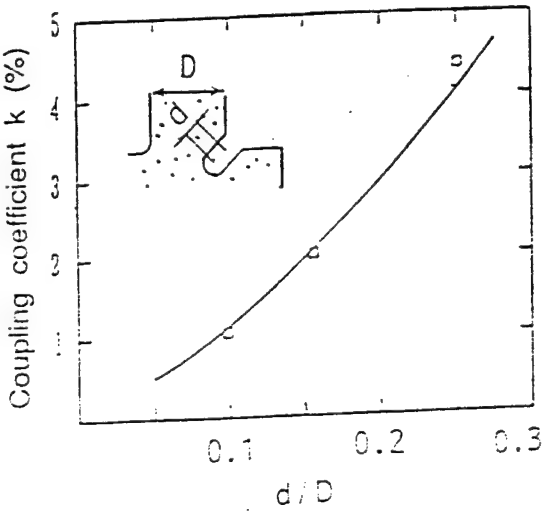

Fig.4 Relation between coupling coefficient and d/D

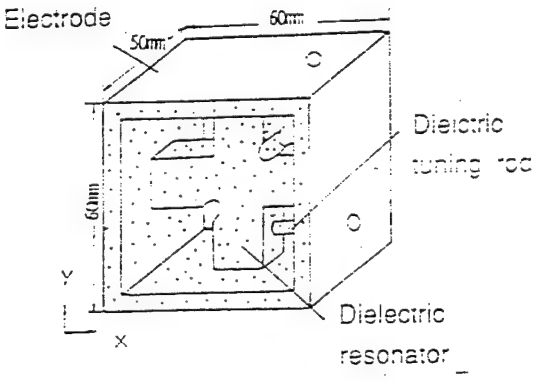

Fig.5 Basic construction of full monoblock type TM_{110} dual mode ASODR

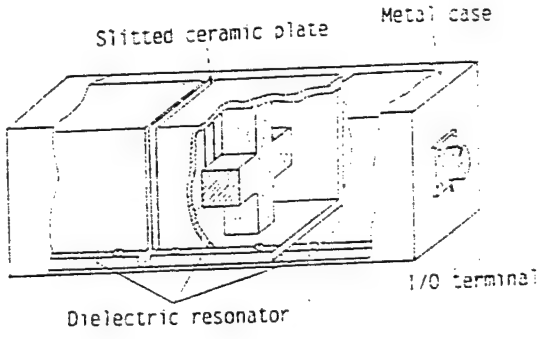

Fig.6 Basic construction of high power bandpass filter using ASODR's

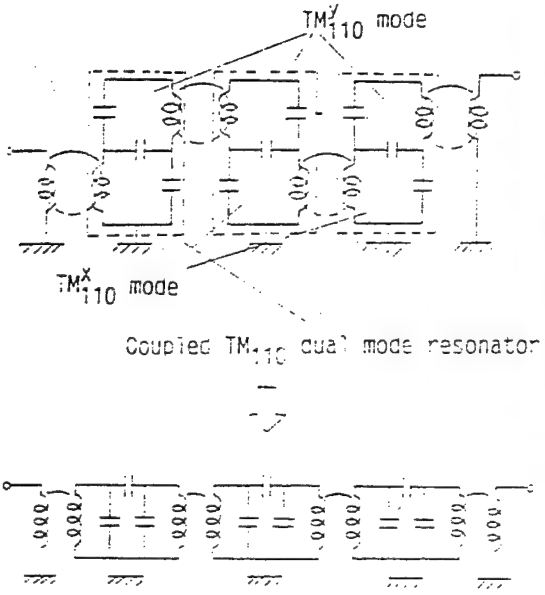

Fig.7 Equivalent circuit of the bandpass filter using ASODR's

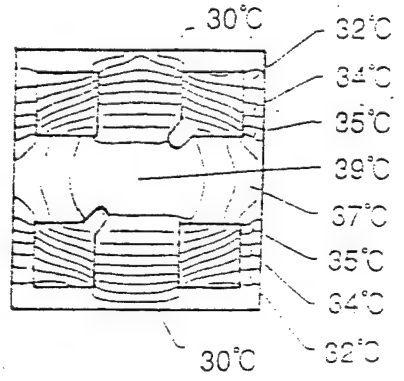

Fig.8 Analytical result of temperature distribution in ASODR

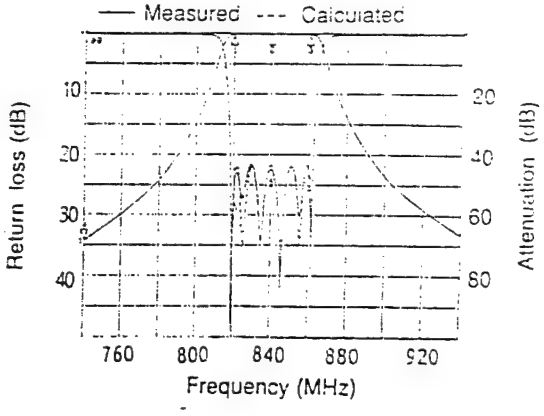

Fig.9 Attenuation and return loss characteristics of the filter

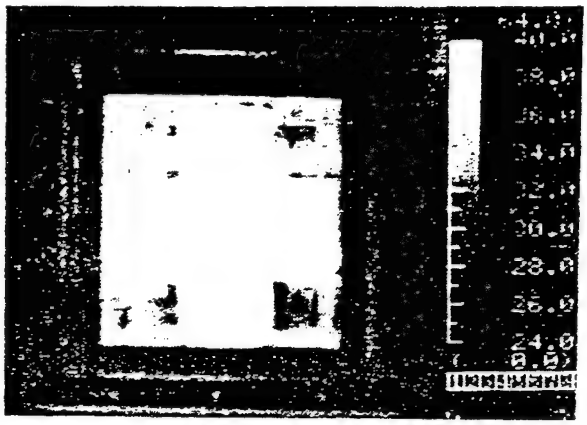

Fig.10 Measured temperature distribution in ASODR

Fig.11 External view of the filter

Center Frequency	840 MHz
Pass Band Width (BW)	40 MHz
Insertion Loss within BW	0.4 dB max.
Return Loss within BW	22 dB min.
Attenuation at $f_c \pm 60$ MHz	46 dB min.
Maximum Input Power	500 Watts
Physical Dimensions	80×90×180 mm

Table 1 Performance of the filter

Resonator Type	Dimensions (mm)	Volume (cm^3)
Reentrant Cavity	90×110×540	5350
TM_{110} single mode	80× 80×350	2240
TM_{110} dual mode	80× 90×180	1300

Note :
Filters in comparison have same performance

Table 2 Comparison of physical size

MOBILE TERMINAL IMPLEMENTATION FOR THE GSM SYSTEM

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Abstract. This paper describes the main results concerning the implementation of a prototype numerical receiver of the future European Cellular System GSM (Group Special Mobile). The proposed Maximum Likelihood Sequence Estimation (MLSE) receiver based on Viterbi algorithm compensates selective distortions due to the multipath propagation and Doppler shifts. The performance of this receiver is evaluated using a channel simulator suitable for mobile communications.

1. INTRODUCTION

The Pan European cellular mobile communication system uses narrow band Time Division Multiplex Access scheme.
The propagation of the electromagnetic field between the fixed station and the mobile unit is affected by many factors, including tropospheric scattering, diffraction from natural and artificial obstacles, topographic and environmental conditions. All these factors lead to the propagation conditions may significantly affect the transmission quality. In particular, the signal quality can be seriously disturbed by the time - varying intersymbol interference introduced by the multipath mobile radio channel.
Section 2 leads off with a brief review of GSM structure and then, in the Section 3, we describe the simulated mobile radio channel implemented considering the following main impairments:

- flat Gaussian noise
- Rayleigh (and Rice) fading with Doppler shift and multiple echoes as representative of different geographical areas.

The Section 4 presents the study and the implementation of an adaptive maximum likelihood Viterbi receiver for signals transmitted via intersymbol interference (ISI) channels.
The receiver is specifically tailored for the application with modulation index $h = 0.5$ and GMSK (Gaussian Minimum shift keying) modulation schemes and well suited for VLSI implementation.
The Section 5 will show the simulation results presented as BER versus a function of the energy bit/noise spectral density E_b/N_0, to evaluate the performance of a TDMA mobile radio system with the proposed MLSE receiver. Moreover the performance in terms of BER after the subsequent decoder block using the Viterbi algorithm are presented.

2. STRUCTURE AND ARCHITECTURE OF THE GSM

In this section the principal characteristics and features of the new generation of the Pan European cellular mobile communication system, called GSM (Group Special Mobile), are described in details.

The communication structure of the GSM system can be supposed as composed by the following main building blocks:

-MS : the Mobile Station;
-BS : the Base Station, to which the MS is connected through a radio link;
-MSC: the Mobile Service Switching Centre; it develops the control functions of the GSM system are concentrated and it is the interface between the fixed network and the GSM network.

The MSC performs all the switching functions required for the management (set-up, clear-down, handover, etc.) of the call to/from the MS.

The main specifications proposed for the GSM system are the following:

- Digital transmission;
- Modulation scheme: Gaussian Minimum Shift Keying (GMSK) with BT = 0.3. The modulation rate is 1625/6 (270.833) kbit/s.
- Frequency bandwidths: 25+25 MHz
  890-915 MHz Mobile transmit, Base receive
  935-960 MHz Base transmit, Mobile receive
- Carrier spacing: 200 kHz, providing 125 available carriers in 25 MHz bandwidth;
- Frequency reuse : 9 groups of carriers for the cellular operation;
- Multiple access: TDMA with 8 channels per carrier.

The TDMA frame is divided in 8 time-slots, each 0.5777 ms long. Each time-slot is reserved to an user to transmit a data packet composed of 148 bits and the structure of the time frames, time-slot and burst is shown in Fig. 1.

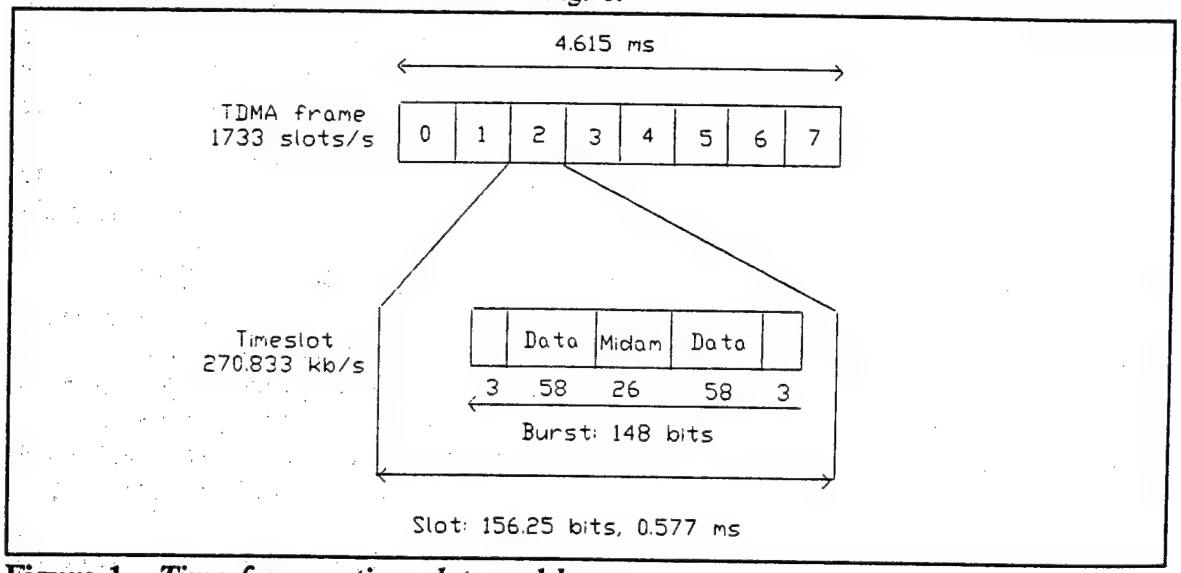

Figure 1 - ***Time frames, time slots and bursts***

The time-slot is a time interval of 0.577 (=15/26) ms, comprising 156.25 bits. Its physical content is called a burst.

There are four types of burst in the system as follows:

NB Normal burst: this is used to carry information on traffic and control channels, it contains 116 encrypted bits and includes a guard time of 8.25 bit duration.

FB Frequency correction burst: this is used for frequency synchronisation of the MS; it is equivalent to an unmodulated carrier, shifted in frequency, with the same guard time as the normal burst; it is broadcast together with the Broadcast Control Channel (BCCH).

SB Syncronisation burst: this is used for time synchronisation of the MS: it contains a long training sequence and carriers the information of the TDMA frame number (FN) and BS identity code; it is broadcast together with the frequency-correction burst.

AB Access burst: this is used for random access and it is characterised by a longer guard time
(68.25 bits or 0.252 ms) to allow for burst transmission from a mobile that does not know the correct timing at the first access (or after handover): this allows for a distance of 35 km from BS.

When the mobile tries to connect with a base station, the FB and SB burst are used.
The MS must synchronise both in frequency and time. The BS sends signals on the BCCH to enable the MS to synchronise itself to the BS and, if necessary, correct its frequency standard to be in line with that of the BS.
Once the link between MS and BS station has been connected, the normal burst is used to transmit the information. The information to be transmitted is coded through a block and a convolutional code and, after, interleaved.

3. MOBILE RADIO CHANNEL

The propagation of the electromagnetic field between the fixed station and the mobile unit is affected by many factors, including tropospheric scattering, diffraction from natural and artificial obstacles, topographic and environmental conditions. All these factors lead to characterize the signal amplitude received at the mobile unit as fading component, due to the reflections from obstacles and the vehicle movement. Generally the assumed model for the envelope of the signal affected by this type of fading is the Rayleigh distribution or the Rice distribution.
Due to the multipath propagation, a transmitted impulse signal produces several replicas at the receiver at different time instants. Therefore, all these features give a representation in terms of time delays and Doppler shifts associated to every path which are shown as:

$$\int\int u(t-\tau)\, S(\tau, f)\, e^{j(2\pi f t)} df\, d\tau \qquad (1)$$

where u (t-τ) are the paths with different delays τ and S(τ,f) Doppler spectrum.
The proposed simplified model is composed by a discrete number of taps, each determined by their time delay and their average power, and by a Rayleigh amplitude varying according to a Doppler spectrum. Each taps are added as showed in Fig. 2.
In the 900 MHz band the delay spread is typically about 0.1μs on flat terrain, 2μs in urban areas and up to 5μs for hilly terrain. The maximum delay can be 0.5μs, 10μs and 20μs in the three environments respectively.
The characteristics of the radio channel can be therefore described by a time-varying impulse response c(τ, t), that is a function of the response delay τ at the current time t.
The shapes of the impulse responses is various in the different propagation conditions and has a relatively long duration.

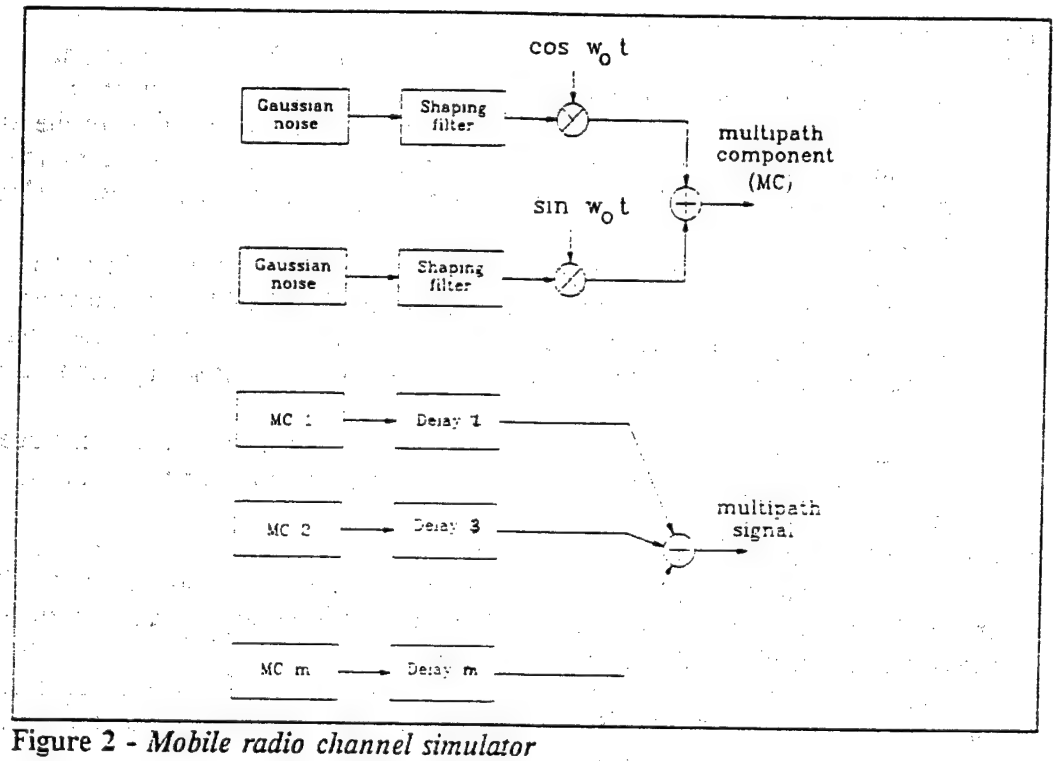

Figure 2 - *Mobile radio channel simulator*

As examples, Fig. 3 shows the equivalent lowpass impulse response of the mobile channel for the urban case.

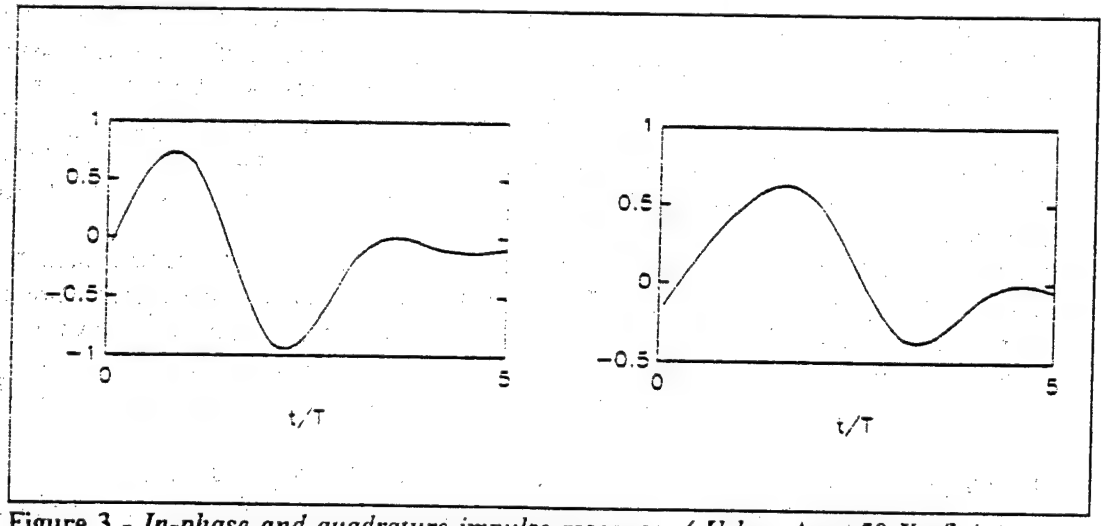

Figure 3 - *In-phase and quadrature impulse response (Urban Area 50 Km/h)*

4. A DIGITAL RECEIVER FOR THE GSM SYSTEM

In this section a prototype digital receiver of the GSM system is shortly described. In the GSM system, the reliability of the digital information is strongly degradated by multipath.

The Maximum Likelihood Sequence Estimation (MLSE) using the Viterbi algorithm seems

one of the most powerful method for the equalization of channels with severe distortions. The Gaussian Minimum Shift Keying (GMSK) modulation can be closely approximated through a linear partial-response QAM signal with the data symbols $a_i = \pm 1$, obtained from the source data symbols by differential encoding, which are phase-rotated in the complex plane by consecutive multiples of $\pi/2$.
Therefore, the transmitted signal is given by

$$s(t) = \sum_{k=-\infty}^{\infty} a_k j^k p(t-kT) \qquad (2)$$

being T the symbol interval and p(t) is a real-valued pulse shaping function.
The QAM model has been extended to cover the effect of linear transmission channels and receiving filters. The received signal y(t) can be given by:

$$y(t)=\sum_k a_k j^k h(t-kT) \qquad (3)$$

where h(t) is the overall complex impulse response of the complete communication system, including the transmitter, the receiver and the channel response.
Applying at the received signal a derotation factor [4] $(-j^k)$ for every i, we obtain a simplified structure of the MLSE receiver.
The general structure of the digital receiver for the GSM system, which has been implemented, is shown in Fig. 4. The received signal y(t) is reported in the base band and sampled at the converter every T.

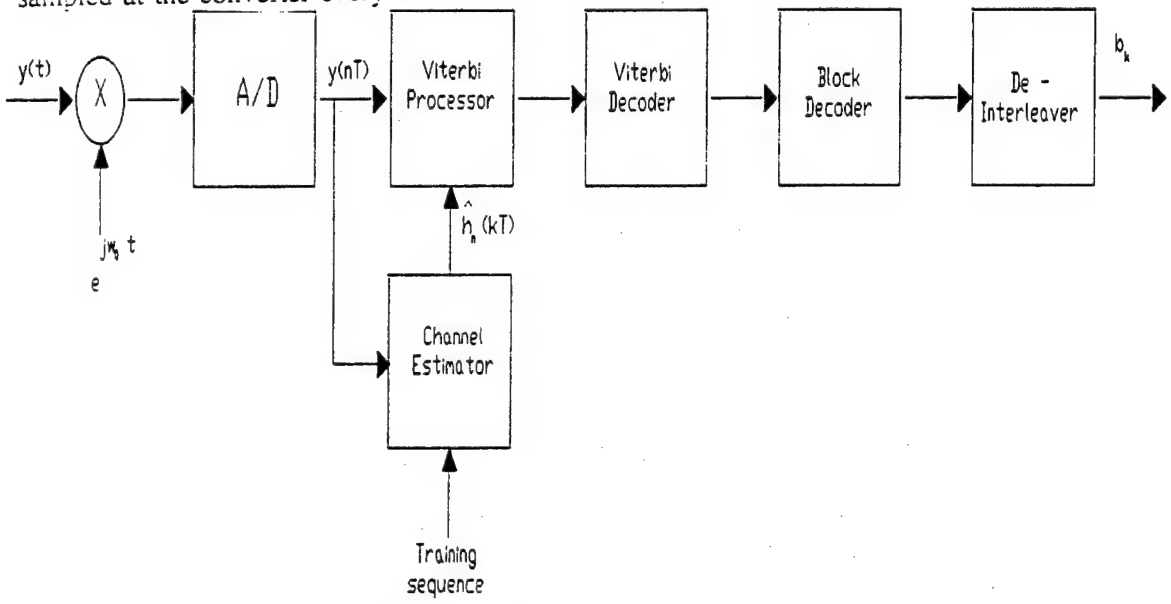

Figure 4 - ***General receiver structure for the GSM system***

In order to recover the source data sequence hidden in the received signal y(t) the MLSE receiver calculates the euclidean metrics for any possible sequence a between the received signal and the reconstructed signal using estimated channel coefficients and searches the particular sequence that minimizes

$$\sum_{i=1}^{M} |y(kT) - \hat{y}(kT)|^2 \qquad (4)$$

where M is the lenght of the whole data symbol sequence.
The Viterbi equalizer requires a good estimation of the actual channel impulse response.
In the GSM system, the data packet contains a pseudo- random sequence of 26 bits, termed midamble, which is known at the receiver. This sequence can be used to perform an estimate of the communication channel during the actual time- slot.
Assuming to take one sample every T and considering that the impulse channel response varies with the time, the signal samples $y_n = y(nT)$ are therefore given by:

$$y(nT) = \sum_k h_n(kT)\ a_{n-k} \qquad (5)$$

The coefficients $h_n(kT)$ are estimated by using the correlation properties of the midamble. To this regard, the channel estimator evaluates the correlation between the received signal samples and the M symbols a_n of the midamble:

$$C_i = \frac{1}{M} \sum_{n=0}^{M-1} \sum_{k=0}^{N} a_n a_{n+1-k}\ h_k \qquad (6)$$

In the pratical implementation of the receiver, the system response have been assumed to span 5 symbols.
The Viterbi algorithm uses the estimated channel coefficients to equalize and demodulate the received symbols. It uses a trellis structure with 16 states and evaluates for each path the Euclidean distance between the received sequence and the reconstructed signal using the estimated impulse response. The Viterbi equalizer gives at its output the sequence having the lowest Euclidean distance and a soft information on each demodulated symbol.
This soft information (3 bits) which gives an estimate of the data reliability, is used in the next block of the receiver that implements the convolutional decoding based also on the Viterbi algorithm.

Furthermore some other considerations are important from the implementation point of view of the digital receiver.

A) The preamble position in middle of the burst allows to produce a channel impulse response estimate that in many situation is sufficiently accurate for the whole duration of the burst even in presence of time-varying multipath fading. For this reason the Viterbi algorithm is initialized at the extremes of the midamble and then works on the informative sequence in direct and inverse propagation. As expected the performance of the receiver is worse at the beginning and at the end of the burst, and only in the case of high speed of the mobile could be necessary to cope with the fast channel response variations by a receiver adaptability (tracking mode).

B) The MLSE receiver only needs the estimate of the channel impulse response $h_n(kT)$ and does not require the knowledge of the carrier phase and of the symbol timing. These information are included automatically in the channel estimate $\hat{h}_n(kT)$. Therefore the MLSE receiver does not require subsystems dedicated to the carrier phase and symbol timing extraction. Moreover even a moderate frequency offset between the carrier frequency and the frequency of the receiver local carrier can be tolerated. The frequency offset appears as a slowly time-varying relative carrier phase

that contributes to the time variations of the channel impulse response.

C) As underlined the value of the parameter N affects the receiver complexity. However, in practice the receiver is robust with respect to the value of N. If turns out that the receiver performance (in terms of error probability) is quite good even for values of N significantly smaller than the actual duration of the channel impulse response. Moreover it turns out that the digital implementation of the MLSE receiver requires short binary register for a satisfactory performance, i.e. the receiver is robust with respect to a finite-arithmetic implementation.

The characteristics outlined above suggest that the MLSE receiver is a good candidate for a digital receiver for mobile communications and is suitable for a VLSI implementation.

5. SIMULATION RESULTS

A computer simulation program has been set up in order to evaluate the performance of a TDMA mobile radio system with the proposed MLSE receiver. The simulation program written in C language runs on VAX station to obtain the BER (bit error rate) performance of the global system.

The following assumption will be made:

- the normalized bandwidth of the premodulation filter in the GMSK transmitter is BT = 0.3 (the bit rate is 1/T= 270.833 kb/s).
- the baseband receiving filter has a 3-dB bandwidth two-sided equal to 160 kHz
- the receiver structure includes a 16 - state Viterbi receiver
- the channel impulse response is estimated every burst and it is used to set at the receiver at the beginning of each time - slot.

The simulated channel impairments are:

- flat Gaussian noise
- Rayleigh fading with Doppler frequency shift and multiple echoes selected by the COST Propagation Group as representative of urban area (TU), rural area (RA) and hilly terrain (HT).

The results of complex echo patterns simulations is reported in Fig. 5 as BER versus E_b/N_0. It can be observed that urban channel is more selective than rural one because includes rather long echo delays.

Also it can be noticed that the bit errors are less in the midamble than in the information message since the channel estimate is evaluated on the note midamble sequence. So, the bit errors grow continuously in the two message parts towards the burst tail.

In Fig.6 is shown the BER versus E_b/N_0 after the Viterbi decoding implementing soft decision.

6. References

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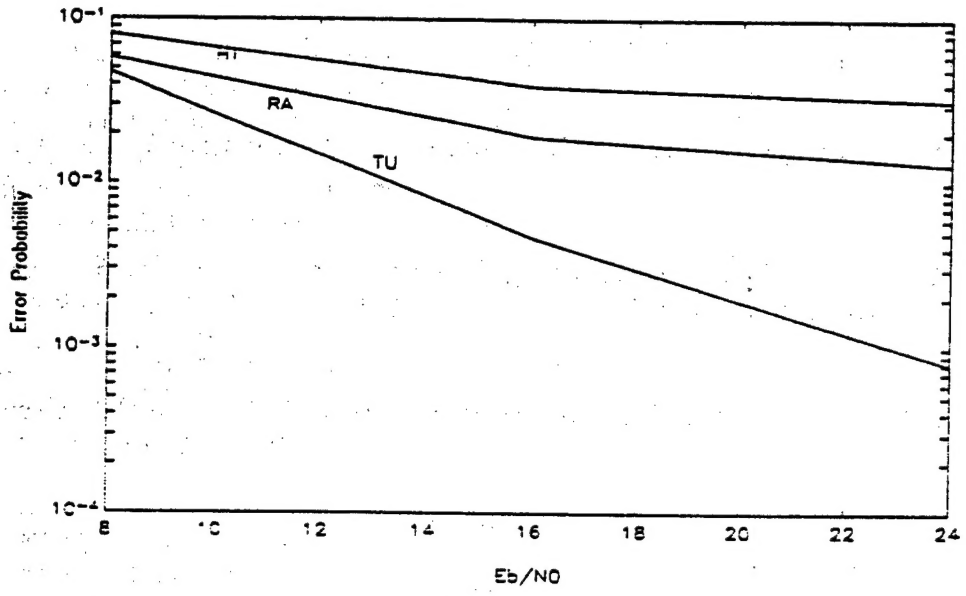

Figure 5 - *Bit error rate performance for the receiver on TU - Urban Area, HT - Hilly Terrain, RA - Rural Area with Doppler velocity of 50 km/h, 100 km/h and 250 km/h respectively*

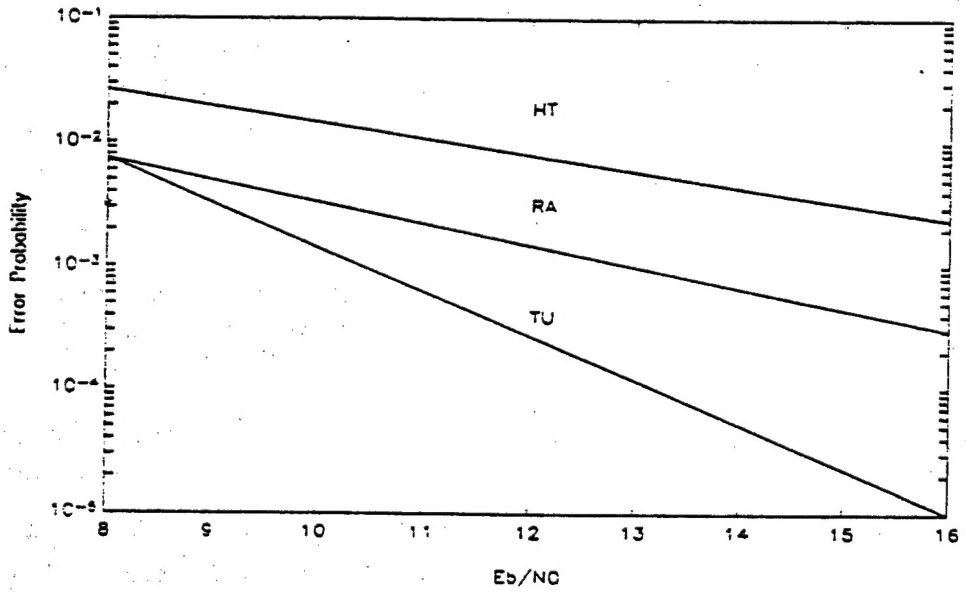

Figure 6 - *BER performance for the Viterbi decoder implementing soft decision in the same above cases*

[3] R. D'Avella. L. Moreno, M. Sant'Agostino, "An adaptive MLSE receiver for TDMA digital mobile radio", IEEE, J. of Selected Areas on Communications, vol. 7, N° 1, p.122-129, January 1989.

[4] A.Baier "Derotation Techniques in Receivers for MSK-Type CPM Signals" Signal Processing,p.1799-1802 1990.

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